

Good Book

INSTRUCTION MANUAL
MODEL 1501A
PROGRAMMABLE PULSE GENERATOR



E-H RESEARCH LABORATORIES, INC.

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INSTRUCTION MANUAL
MODEL 1501A
PROGRAMMABLE PULSE GENERATOR

Serial No.

February 1976

INSTRUCTION MANUAL
MODEL 180TA
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148-07205B

INSTRUMENT WARRANTY

All E-H/AMC products are warranted for a period of one year from date of delivery. These products are warranted to be free from defects in material and workmanship, suitable for normal use and service under normal conditions, and able to meet any applicable specifications accepted in writing by E-H/AMC. No claim under the warranty will be accepted unless it is made in writing to E-H/AMC immediately after discovery of defect or in any case, within one year of delivery. No other warranty, express or implied exists outside this warranty. E-H/AMC is not liable for any commercial losses or other consequential damages incurred or sustained as a result of any defective or nonconforming product. E-H/AMC's obligation with respect to losses is limited, under this warranty, at E-H/AMC's option, either to the replacement (by delivery F.O.B. Oakland, California) or repair of its manufactured products which prove to be defective or nonconforming. This warranty does not apply to any products improperly applied or used or which have been subjected to intentional or negligent misuse or accident, or which have been in any way modified by others without the express written agreement of E-H/AMC. Any product claimed to be defective during the warranty period must be returned to an authorized E-H/AMC repair center, with transportation charges prepaid. The product will be repaired and returned to the purchaser with return transportation prepaid by E-H/AMC. If no defect in the product is found, or if failure is due to misuse or accident, such product will be returned to the purchaser with repair and transportation charges billed collect.

For in-warranty repair of this instrument, contact E-H Research Laboratories, Inc., Customer Service Department and provide:

- a. Instrument model number and serial number.
- b. Details concerning the nature of the malfunction.

Shipping instructions, or repair information and parts will be sent to you promptly.

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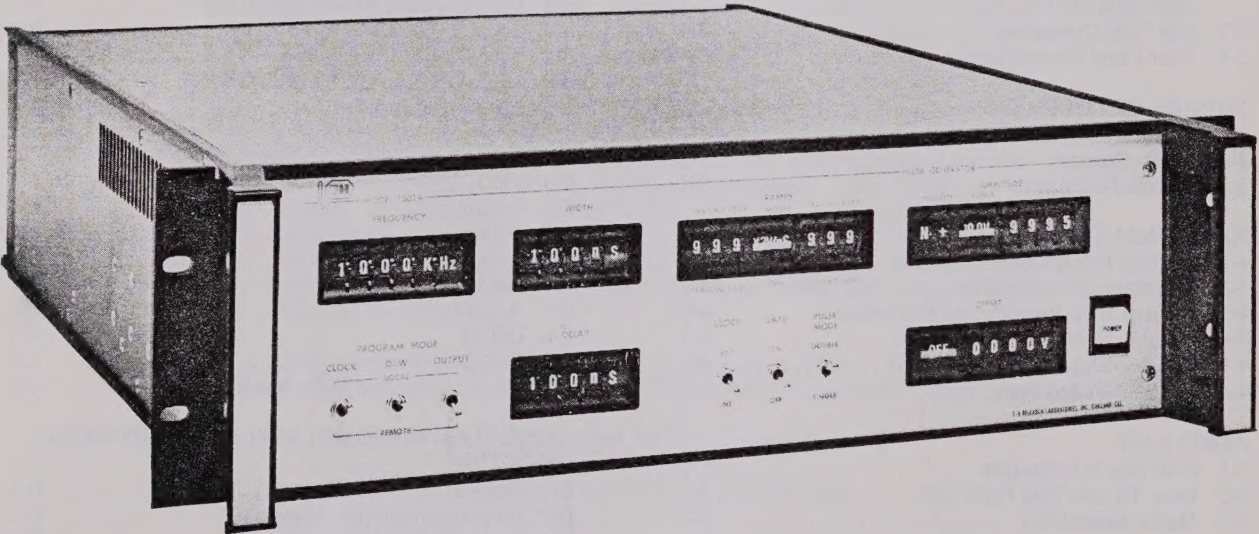


Figure 1-1 Model 1501A Programmable Pulse Generator
(with Optional Front Panel Controls)

SECTION 1

SPECIFICATIONS

1-1 HOW TO USE THIS INSTRUCTION MANUAL

This manual is divided into two basic sections. The first section provides information for the “basic” Model 1501A with parallel BCD programming. This section also contains maintenance information and parts lists for the common, pulse-generating portions of the Model 1501A. The second section of the manual provides appendices covering the various programming options. Information for front-panel control options is also included in an appendix.

To find the information pertaining to your unit, use the following list to determine which appendix to use.

Option	Description	Appendix
01-PON	Parallel BCD, negative true	Basic Manual
01-AON	ASCII, negative true	Appendix A
01-SON	16-bit serial, negative true	Appendix B
01-SOPI	Serial-by-Word Isolated	Appendix D
01-UON	Universal Instrument Bus	Appendix E
02	Front-panel controls	Appendix C
03	Bench mount	Basic manual
04	Chassis Slides	Basic manual
05	Extender boards	Basic manual

Options 03 through 05 are mechanical options which do not affect operating or maintenance information. Parts lists found in Section 5 of the basic manual will provide information for options 03, 04, and 05.

1-2 GENERAL INFORMATION

The E-H Model 1501A Programmable Pulse Generator is a compact unit designed to meet the requirements for a fully programmable pulse generator in high-speed, automatic test system applications. Programmable 10 V output amplitude, and 50 MHz repetition frequency capabilities make the Model 1501A an ideal choice for any application requiring TTL and DTL drive sources.

Full control of all pulse parameters is provided by external parallel programming lines. Interface to integrated circuits and adaptation to current logic levels is enhanced by the addition of variable baseline offset and polarity inversion functions, which allow simulation of positive, negative or inverted logic. Baseline offset is inserted after the attenuator to permit full use of the offset capability.

Synchronous and asynchronous gating are provided as useful features for systems applications. Distortion is less than 5% peak-to-peak for all functions.

Normal/inverted and single/double pulse modes are built into the Model 1501A. In the inverted mode an extremely high duty cycle can be achieved for the output pulse.

1-3 SPECIFICATIONS (all specifications assume a 50-ohm resistive load on the output). (See also subsection 1-4, Accuracy).

a. **Pulse Repetition Frequency.** From 0.5 Hz to 50 MHz in 8 decade ranges.

b. **Pulse Delay.** From 10 ns to 1 s in 8 decade ranges.

c. **Pulse Width.** From 10 ns to 1 s in 8 decade ranges.

d. **Jitter.** Less than 0.1% of setting applies to frequency, delay, or width jitter.

e. **Duty Factor.** Greater than 50% applies to either delay or width circuit.

f. **Modes.** Normal/Inverted and Single/Double Pulse. The inverted mode allows an extremely high duty cycle for the output pulse.

g. **External Drive.** Input drive signal must go from less than 0.75V to greater than 1.5V into a 300-ohm load. Maximum input 5V. Maximum frequency 50 MHz.

h. **Synchronous Gate.** Input drive signal must go from less than 0.75V to greater than 1.5V into a 375-ohm load. Both gate on and gate off modes are under program control.

i. **Asynchronous Gate.** Input drive signal must go from greater than 2.5 V to less than 0.75 V into a 50 ohm load. Gate off operation only.

j. **Trigger Output.** Greater than +1.5V into 50 ohms; greater than +3V into high impedance. Width 10 to 100 ns depending on frequency. Two additional clock outputs available for master/slave pulse generator operation. Output levels same as trigger output. Clock outputs are nominally 25-30 ns early with respect to trigger output.

k. **Minimum Double Pulse Spacing.** Less than 12% of width range maximum.

l. **Amplitude.** ± 39 mV to ± 10 V into 50 ohms from a 50-ohm source. Attenuator accuracy is $\pm 2\%$.

m. Offset. 0 to $\pm 5V$ ($\pm 50mV$) into 50 ohms independent of attenuator setting. The maximum output amplitude is restricted to $\pm 10V$ for the sum of the pulse and offset amplitudes when driving a 50 ohms load. In the off position offset is less than $\pm 10mV$.

n. Pulse Distortion. Less than 5% peak-to-peak for all amplitudes and for all rise and fall times greater than 3 ns.

o. Rise and Fall Time. Less than 3 ns to 0.8 ms in 6 decade ranges. Separate rise and fall verniers.

p. Ramp Linearity. Less than $\pm 1.5\%$ above 100 ns. Less than $\pm 5\%$ 10 to 100 ns.

1-4 ACCURACY (Including all programming options)

a. Repeatability. $\pm 1\%$ of setting.

b. Programming Error. $\pm 5\%$ of desired value for amplitude, frequency and offset; $\pm 5\% \pm 3$ ns for rise and fall times. $\pm 5\%$ of value for delay and width except $\pm 15\%$ of value for 10 ms–100 ms and 100 ms–1 s ranges. Delay and width relate to fastest ramps.

c. Settling Time. Less than 2.5 ms for attenuation and polarity; less than 750 μs when going to or from ramp ranges 0 and 1.

1-5 PROGRAMMING FORMAT (Option 01-PON only)

a. Digital Control Lines. Four range and mode control lines and 12 vernier control lines for each function.

b. Logic Levels. Logic “1” less than 0.75 V; logic “0” greater than +2.5 V, 5V maximum. Each program line is equal to one 7400 TTL load. Positive true logic (Option 01-POP) supplied on request.

c. Programming Format. Four bits define mode and range and 12 bits define vernier information in a three digit BCD format.

Programming formats for other options are discussed in the appendices for each option.

1-6 MISCELLANEOUS

a. Dimensions. 5- $\frac{1}{4}$ in. (13.3 cm) high, 19 in. (48.2 cm) wide, 20- $\frac{3}{4}$ in. (52.7 cm) deep.

b. Weight. 35 lb. (15.9 kg).

c. Power Requirements. 100, 117, or 230 VAC $\pm 10\%$, 50-60 Hz, approximately 200 VA.

d. Operating Temperature Range. 0°C to +55°C.

e. Temperature Coefficient of pulse parameters.

Frequency	.	.	.	.	$\pm 0.3\%/degree\ C.$
Width and Delay	.	.	.	.	$\pm 0.1\%/degree\ C.$
Amplitude	.	.	.	.	$\pm 0.05\%/degree\ C.$
Offset	.	.	.	.	$\pm 0.05\%/degree\ C.$

SECTION 2 OPERATING INFORMATION

2-1 GENERAL INFORMATION

This section of the Instruction Manual gives installation procedures, and describes the operating controls and modes of operation.

The Performance Verification Procedure given in Section 4 of this manual serves as a receiving inspection. All of the operating controls are shown on the Block Diagram in Section 3 in relation to the functional elements of the instrument. Specifications from Section 1 which directly affect operation of the instrument are reiterated in this section.

2-2 INITIAL INSPECTION AND INSTALLATION

a. Unpacking. Unpack the instrument and verify that it is intact and as ordered. Ensure that any accessories (as listed at the end of Section 1) that should accompany the instrument are present. Inspect the instrument for any physical damage. If damage of any sort is found, a claim should be filed immediately with the carrier. As soon as possible, the instrument should be given a thorough electrical inspection. The Performance Verification Procedure given in Section 4 is recommended for this purpose. If the instrument fails to operate properly or does not meet specifications, contact an E-H Representative.

NOTE

Unauthorized repair or parts replacement during the warranty period may void the warranty. The warranty and instructions for in-warranty repair of this instrument are given on Page ii of this manual, opposite the Table of Contents.

b. Installation. The E-H Model 1501A is supplied in a rack-mount configuration. Refer to Figure 2-1 for mounting dimensions. Power connection and fuse requirements are silk-screened on the rear panel. Input ac power is connected via the three-conductor power cord (supplied) to rear panel connector J101. The POWER switch should be turned OFF (down) prior to plugging in the instrument. The instrument is cooled by an internal fan that operates when the POWER switch is turned ON. The top and bottom covers should remain in place when the instrument is in use to provide proper flow of cooling air.

2-3 DESCRIPTION OF CONTROLS AND CONNECTORS

a. Front Panel Controls. The sole front-panel control is POWER switch S201, which controls primary power to the instrument. Rear-panel fuses are provided.

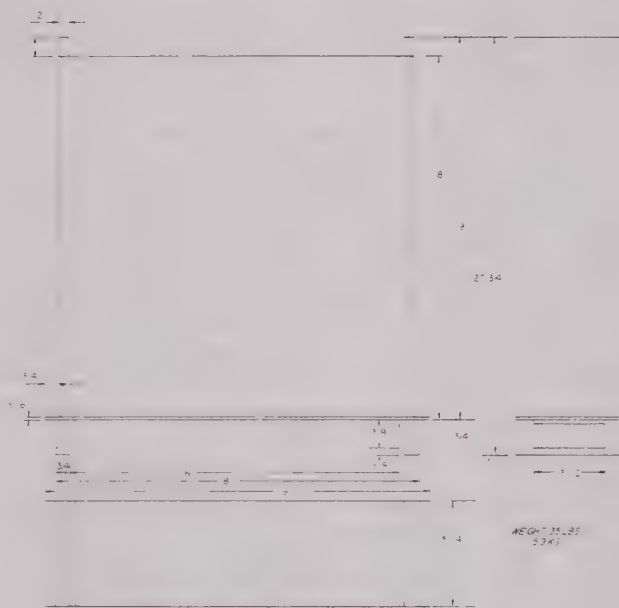


Figure 2-1 Outline and Mounting Dimensions

b. Rear Panel Connectors (Refer to Figure 2-2)

(1) Trigger Output. Greater than +1.5 V into 50 ohms; greater than +3 V into high impedance. Width 10 to 100 ns depending on frequency. Two additional clock outputs available for master/slave pulse generator operation. Output levels same as trigger output. Clock outputs are nominally 25-30 ns early with respect to trigger output.

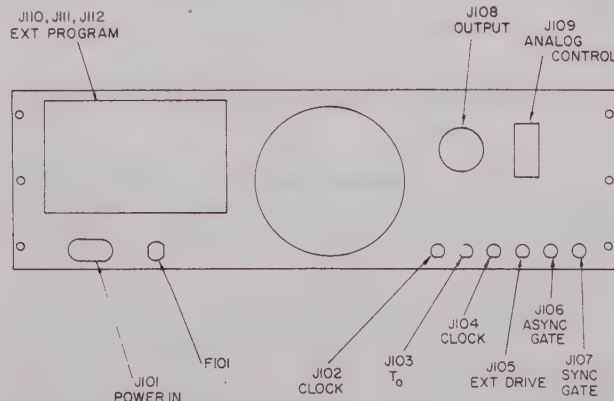


Figure 2-2 Rear Panel Connectors

(2) External Drive Connector. The input drive signal must go from less than 0.75 V to greater than 1.5 V into a 300-ohm load. Maximum input 5 V. Maximum frequency 50 MHz.

(3) Asynchronous Gate In. The input drive signal must go from greater than 2.5 V to less than 0.75 V into a 50 ohm load. Gate off operation only.

(4) Synchronous Gate In. The input drive signal must go from less than 0.75 V to greater than 1.5 V into a 375-ohm load. Both gate on and gate off modes are under program control.

(5) Pulse Output. ± 39 mV to ± 10 V into 50 ohms from a 50-ohm source.

2-4 PROGRAMMING INFORMATION - Option 01 P0N

a. **General.** Model 1501A programming can be divided into three parts: Range, Mode, and Vernier. Range control is coded in a 4-2-1 format (three binary lines); vernier is coded in a three-digit BCD format (8-4-2-1) with a total of 12 lines per vernier. Mode control is a single-line on/off format, providing such functions as internal/external clock, normal/inverted pulse, etc. All control lines have inputs equal to one 7400 series TTL load. All lines are programmed with negative true logic, where logic "1" is equal to 0 V.

b. **Vernier Programming.** Each set of vernier connections is made up of three digits in 8-4-2-1 BCD form. See Table 2-4. Width and delay programming is straightforward: the number programmed in BCD form is the required value. For example, a pulse width of 172 μ s is a vernier value (in BCD) of 172. Frequency, amplitude, and offset require transformation from the desired value to the correct vernier. These functions will be discussed in the following paragraphs.

c. **Frequency Programming.** Because the frequency ranges do not have end points which are even decades, the required vernier is found by multiplying the desired frequency by a factor of two and taking the three most significant digits as the vernier. For example, a pulse repetition frequency of 452.3 kHz multiplied by two gives a value of 904.6 and a vernier program of 905.

d. **Amplitude Programming.** The basic (unattenuated) amplitude range is 5 V with 000 vernier and 9.99 V with 999 vernier. To determine the vernier for a given amplitude, including attenuation, use the formula below:

$$\text{Ampl. Vernier} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005}$$

e. **Offset Programming.** The range of offset programming is from 0 to 5V. The vernier program is the required offset value in volts, multiplied by 200. For example, if the required offset is 200 mV, the vernier is 200 x 0.2, or 040.

f. **Leading and Trailing Edge Ramps.** Since the leading and trailing edge ramps of the Model 1501A are constant slope with respect to changes in amplitude vernier, and constant risetime with respect to changes in attenuation, a calculation must be made to determine the program for a given combination of amplitude and rise/fall time. The *fastest* leading and trailing edge times are obtained at a vernier of

999, and the *slowest* times at a vernier 100. To determine the proper vernier, use the following formula:

$$\text{Ramp Rate} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{rise or fall time}}$$

where "K" = .8 for 10-90%, K = .6 for 20-80%, etc.

SAMPLE PROGRAM

Required Amplitude: 800 mV

Required 10-90% risetime: 20ns

Step 1. Determine attenuation value by inspecting Table 2-1. An 800 mV output will be obtained on Range 4 which has an attenuation value of 8.

Step 2. Set attenuator to Range 4.

Step 3. Determine amplitude vernier setting using the attenuation value found in Step 1.

$$\begin{aligned} \text{Ampl. Vernier} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005} \\ &= \frac{(.800 \times (8)) - 5}{.005} \\ &= 280 \end{aligned}$$

Step 4. Set Amplitude vernier to 280.

Step 5. Determine ramp rate using:

$$\begin{aligned} \text{Ramp Rate} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{risetime}} \\ &= \frac{(.800) \times (8) \times .8}{20 \text{ ns}} \\ &= \frac{5.12 \text{ V}}{20 \text{ ns}} \\ &= \frac{5.12 \text{ V}}{.02 \mu\text{s}} \\ &= 256 \text{ V}/\mu\text{s} \end{aligned}$$

By inspecting Table 2-1, we find that a ramp rate of 256 V/ μ s can be obtained with Ramp Range = 1.

Step 6. Set Ramp Range to 1.

Step 7. Set Ramp vernier to 256.

NOTE

Since the vernier only varies between counts of 100 to 999, it may be necessary to multiply the Ramp Rate by either 10 or 100 to obtain the three-digit vernier setting. Example: if Ramp Rate = 24 V/ μ s, then Vernier = 24 x 10 = 240. Example: if Ramp Rate = 1.3 V/ μ s, then Vernier = 1.3 x 100 = 130.

g. **Range Programming.** Table 2-1 lists range values.

h. **Programming Connections.** Tables 2-2 through 2-4 list required connections to rear-panel connectors.

2-5 OPERATING NOTES

The risetime of the Model 1501A output pulse has appreciable frequency components up to 500 MHz. If any of the connectors, cables, or attenuators used do not have flat responses in excess of 500 MHz, degradation of pulse risetime will result. Mismatch effects can also degrade the pulse shape. When possible terminate the output of the 1501A into a 50-ohm pure-resistive load. If the input impedance of the device or system under test is other than 50 ohms, use an impedance matching device to minimize the mismatch effects.

(1) **Open Circuit Operation.** The maximum output amplitude shall be greater than ± 19.5 V peak-to-peak as measured into a load resistance $> 5K$ ohms. The maximum absolute voltage level from ground shall be limited to 14 volts at minimum offset. 1.5 times the offset voltage is subtracted from the 14 V limit for offsets of the same sign as the output pulse, and the value of the offset is added to the 14 V limit for offset of opposite polarity.

2-6 BRIEF DESCRIPTION OF MODEL 1501A OPERATING MODES

Ext. Clock (J110-33)

Bringing this line to ground disables the internal frequency circuits (clock) and enables an external trigger signal applied to J105 to control the Model 1501A pulse output frequency from 0 to 50 MHz. Trigger signal is generated for each input to J105 and is available at the normal trigger output connector, J103.

Dbl. Pulse (J110-41)

Grounding this line allows pulse pair operation. The first pulse is roughly coincident with the trigger output—the second pulse is spaced by using the DELAY programming. This mode usable with either internal or external clock.

Normal Pulse (J110-49)

Grounding this line gives a pulse whose baseline is at the OFFSET level programmed and whose pulsetop is at the AMPLITUDE level programmed (see below).

Gate On (J111-33)

Grounding this line allows a signal (or DC level) connected to J107 to gate on the Model 1501A output. In this mode, both internal clock and output circuits are disabled until gated on. When line is ungrounded (high level), gate off signal applied to either Asynchronous or Synchronous gate inputs turns off output. In Asynchronous mode, internal clock runs and trigger signals are generated. When gate signal goes high in Asynchronous mode, first output pulse occurs at next clock period.

Pos. Polarity (J111-49)

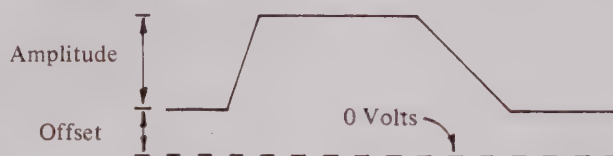
When this line is grounded, the leading edge of the pulse moves in a positive direction in normal mode; when the line is ungrounded, the leading edge of the pulse moves in a negative direction in normal mode.

(B)

+Offset (J112-19) and -Offset (J112-8)

These lines control whether baseline offset is positive with respect to ground or negative with respect to ground.

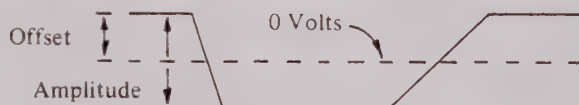
Positive Normal Pulse



Positive Inverted Pulse



Negative Normal Pulse



Negative Inverted Pulse



2-7 234 VOLT OPERATION

a. **General.** The Model 1501A power transformer primary is normally connected for 117 V service. For use with 234 V service, the primary must be reconnected. This is accomplished by altering the input connections and jumpers on the ac input terminal strip, TS101. Proper connections for either type of service are shown on the Primary AC Power schematic in Section 6.

b. Reconnection Procedure

(1) Check the rear panel "Power Data" chart to determine the existing power connection.

(2) Disconnect the power cord and remove the bottom cover using the procedure given in Section 4-4.

(3) Locate TS101 on the bottom chassis layout drawing in Section 6.

(4) Remove the terminal strip cover and position the jumpers, as shown on the power supply schematic, for the type of service desired.

(5) Replace the bottom cover on the instrument. Note the change in power connection on the rear panel "Power Data" chart. Change the line fuse, F101, to correspond with the power connection.

2-8 REAR PANEL CONNECTORS

The following is a summary of the input and output connectors located on the rear panel of the Model 1501A.

J101	. . .	AC Primary Power Input
J102	. . .	. . . Clock Output
J103	. . .	. . . Trigger (T_o) Output
J104	. . .	. . . Clock Output
J105	. . .	. . . External Drive Input
J106	. . .	. . . Asynchronous Gate Input

J107	. . .	Synchronous Gate Input
J108	. . .	. . . Pulse Output
J109	. . .	. . . Not Used
J110/111/112/113	. . .	Programming Input/Output (Serial Program Units Only)
J110/111/112	. . .	. . . Programming Input (Parallel Program Units Only)

See timing diagram, Figure 2-3, for time relationships.

Figure 2-3 Timing Diagrams

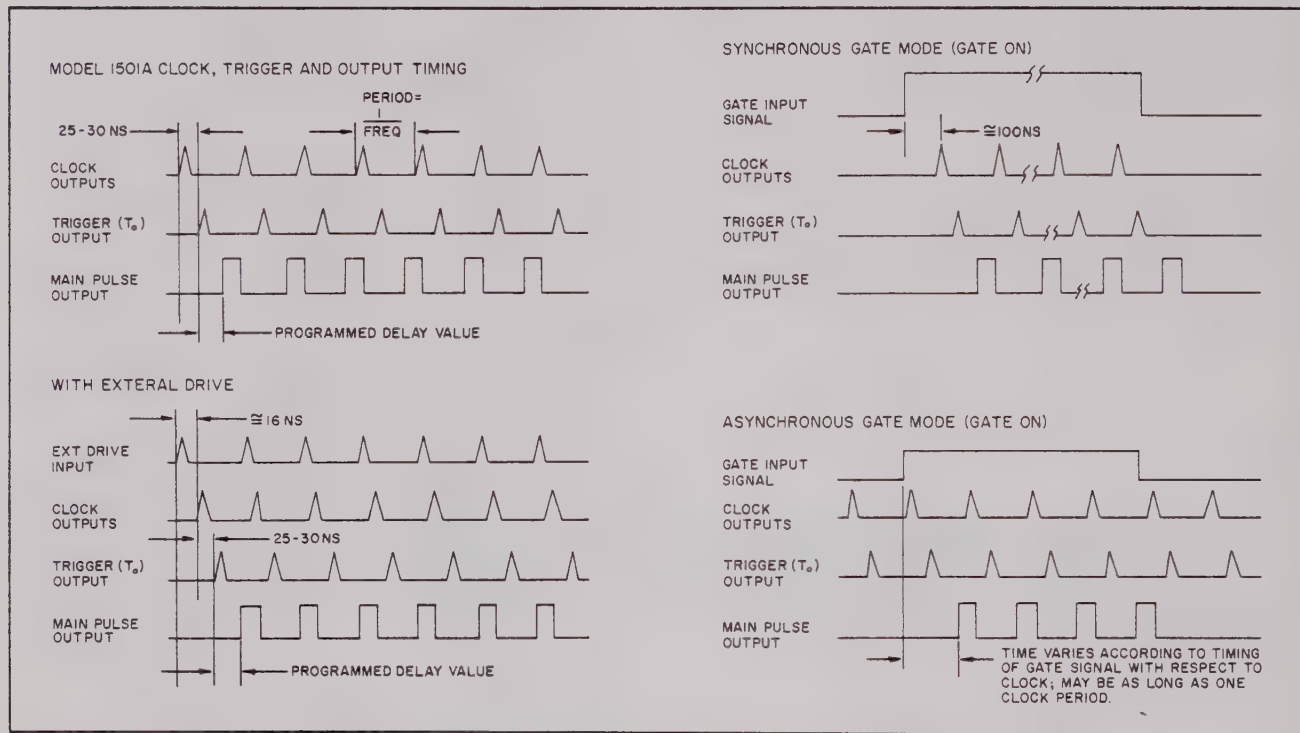


Table 2-1 Range Programming

Function	Range Value	Range	Vernier
Frequency	0	0.5 Hz-4.995 Hz	
	1	5 Hz-49.95 Hz	
	2	50 Hz-499.5 Hz	
	3	500 Hz-4.995 kHz	
	4	5 kHz-49.95 kHz	
	5	50 kHz-499.5 kHz	
	6	500 kHz-4.995 MHz	
	7	5 MHz-49.95 MHz	
Delay/Width	0	10 ns-99.9 ns	100-999
	1	100 ns-999 ns	100-999
	2	1 μ s-9.99 μ s	100-999
	3	10 μ s-99.9 μ s	100-999
	4	100 μ s-999 μ s	100-999
	5	1 ms-9.99 ms	100-999
	6	10 ms-99.9 ms	100-999
	7	10 ms-999 ms	100-999
Ramp Rate	0	uncalibrated range*	100-999
	1	0.1-0.999 V/ns	100-999
	2	10.0-99.9 V/ μ s	100-999
	3	1.0-9.99 V/ μ s	100-999
	4	0.1-0.999 V/ μ s	100-999
	5	10.0-99.9 V/ms	100-999
Attenuation	0	(x 128) 40-80 mV	000-999
	1	(x 64) 80-156 mV	000-999
	2	(x 32) 156-312 mV	000-999
	3	(x 16) 312-625 mV	000-999
	4	(x 8) 0.62-1.25 V	000-999
	5	(x 4) 1.25-2.5 V	000-999
	6	(x 2) 2.5-5.0 V	000-999
	7	(x 1) 5.0-10.0 V	000-999

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table 2-2 Range Programming Connections

BCD Value	Frequency J110 pin	Delay J110 pin	Width J110 pin	Ramp J111 pin	Atten J111 pin
4	8	16	24	8	24
2	32	40	48	32	48
1	7	15	23	7	23

Table 2-3 Mode Programming Connections

Mode	Pin
Ext. Clock	J110-33
Dbl. Pulse	J110-41
Normal Pulse	J110-49
Gate On	J111-33
Pos. Polarity	J111-49
+ Offset	J112-19
- Offset	J112-8
Ground	J110-25, 50
	J111-25, 50
	J112-9, 10, 21, 22

Table 2-4 Vernier Programming Connections

BCD Value (1-2-4-8)	Freq. J110 pin	Delay J110 pin	Width J110 pin	Trlg. Edge J111 pin	Ldg. Edge J111 pin	Ampl J111 pin	Offset J112 pin
800	31	39	47	39	31	47	18
400	6	14	22	14	6	22	6
200	30	38	46	38	30	46	17
100	5	13	21	13	5	21	5
80	29	37	45	37	29	45	16
40	4	12	20	12	4	20	4
20	28	36	44	36	28	44	15
10	3	11	19	11	3	19	3
8	27	35	43	35	27	43	14
4	2	10	18	10	2	18	2
2	26	34	42	34	26	42	13
1	1	9	17	9	1	17	1

SECTION 3

THEORY OF OPERATION

3-1 GENERAL INFORMATION

The following section of this manual contains an electrical description of each of the circuits of the E-H Model 1501A Programmable Pulse Generator. The description is divided into two parts. The first part is a discussion of the block diagram for the instrument, and the second part is a detailed discussion of each of the circuits which comprise this instrument.

3-2 BLOCK DIAGRAM (Refer to Figure Number 3-1)

The E-H Model 1501A Pulse Generator is basically identical to any conventional laboratory pulse generator with the addition of appropriate digital or analog programming circuits. The clock multivibrator, which determines the base repetition frequency for the instrument, operates in the frequency range of 5 to 50 MHz. The actual operating frequency is determined by the signal which is supplied by the digital-to-analog converter or by an external analog program level. All of the remaining clock ranges are generated by dividing the 5 to 50 MHz frequency range by an appropriate value in the divide by 10^n counter. For example, the 0.5 hertz to 5 hertz range is obtained by dividing the basic clock frequency range by 10^7 . The output of the divider is supplied to the input of a buffer amplifier to drive the width and delay circuits and to a trigger driving amplifier which supplies the trigger output pulse from the Model 1501A.

Also associated with the basic clock multivibrator is the synchronous gating circuitry. These circuits provide for synchronously gating the clock on or gating the clock off from a positive going gate signal selected by program control. In cases where external drive is preferred, program control can substitute the output of the external input circuit for the clock circuit.

A second gating circuit is supplied at the input of the delay and width module. This gate is of the asynchronous type.

The delay one-shot operates in decade ranges from 10 nanoseconds down to 1 second. The absolute delay within any given range is determined by the setting of the D to A converter or external analog program. The ranges are determined by the data supplied to the buffer card whose output causes an appropriate range capacitor and charging current to be selected for each of the six ranges. The delay one-shot's output drives through a set of gates the width one-shot which has identical ranges and operates in the same manner as the delay one-shot.

These gates provide for double pulse operation by supplying both the normal and inverted output of the delay multivibrator to the input of the width multivibrator. This

causes the width one-shot to trigger on both the leading and trailing edges of the delay one-shot. The output of the width one-shot is amplified and/or inverted by the pulse logic circuit under program control. When the output pulse is to be complemented, the circuit simply inverts the output of the width one-shot providing the appropriate drive form for the output. In the output module the signal is first shaped and amplified and then presented to the input of the ramp generator.

The ramp generator provides five calibrated and one uncalibrated ranges of ramp speed. Each range controls both the leading and trailing ramp rate. However, there are individual D to A cards for the leading and trailing edges of the ramp signal. The output of the ramp drives a quasi-linear amplifier that supplies the needed amplification and also provides the necessary amplitude control. This amplifier drives the junction of a polarity switch and the back match.

The polarity switch consists of a balun and relay combination which drives the output attenuator. This, in turn, supplies attenuation values of unity transfer for an attenuation ratio of 128 to 1 in binary steps under program control. At the output of the attenuator the offset signal, which is derived from the setting of the D to A converter card or from an external program source, is combined with the pulse generator's output in a current summing technique. The resulting output pulse is supplied to the rear panel of the Model 1501A as the output signal.

3-3 CIRCUIT DESCRIPTION

a. **General.** Each of the functional blocks of the block diagram is described in detail in the following paragraphs. The following definitions are utilized in this discussion.

(1) **Vernier Input.** A vernier input is a signal which is either a voltage in the range of 0 to 5 Volts, or a signal resulting from connecting a resistor of 0 to 10,000 ohms to the input in question. All vernier inputs are directly proportional to the parameter they control.

(2) **Range Input.** The range input consists of three digital control lines which are programmed in octal fashion.

(3) **Functional Input.** A functional input is a single binary line that controls such parameters as positive or negative output pulse, single or double pulse mode, etc.

(4) **Logical 1.** A logical 1 is the signal level between 0 and 0.5 Volts.

(5) **Logical 0.** A logical 0 is a signal level between 2.5 and 5 Volts.

b. Type B Clock Module. The basic clock multivibrator is composed of transistors Q4 and Q5 and their associated circuitry. This multivibrator is of the conventional emitter coupled form whose collector resistor has been replaced by clamping diodes CR21, and CR22, CR23, and CR24 and current source transistors Q23 and Q24. The charging current for the timing capacitor C4 is supplied by the current source, Q2 and Q3. These transistors are programmed through an input buffer amplifier with transistors Q11 through Q13 providing the vernier control of the clock frequency. Since the capacitor charging current relates directly with frequency, this clock programs frequency directly. The current supplied to the timing capacitor has approximately a 10 to 1 variation from roughly 2 or 2-1/2 mils to 20 or 25 milliamps. In order to cover this range and maintain proper circuit action, the current sources in the collector of the multivibrator must track the timing current sources. This is accomplished via transistor Q1 which, through emitter follower Q25, drives the collector current sources, which supply the appropriate bias currents to the collector of the multivibrator, transistors Q4 and Q5.

Diodes CR21 and CR24 clamp the collectors to a maximum negative excursion of approximately 400 millivolts while diodes CR22 and CR23 provide a positive clamp that is roughly +600 millivolts, thus allowing a 1 Volt collector swing on the clock multivibrator. The reference voltage supply for this positive clamp is controlled by potentiometer R68 which functions as an overall range adjusting potentiometer. Transistor Q26 shifts the bias point of the voltage source for diodes CR22 and CR23 to compensate for the changes in the clamp diodes due to changing operating points. The magnitude of this correction is controlled by potentiometer R53. Potentiometer R26 provides compensation for general circuit non-linearities that occur near the low frequency end of the vernier range.

The output of the clock, which is taken from buffer transistors Q9 and Q10, drives the count down amplifier Q14, Q15, and Q18, and the buss driver Q29 and Q30. The output of the count down amplifier drives a series of decade counters (ICs 1 through 7) which divide the basic clock frequency by any power of 10 from 0 through 7. The operation of this circuit can be described by a simple example. Assume that we wish to be in the frequency range of 50 to 500 kilohertz. Hence, we wish to divide the basic clock frequency by 100. To do this the range input is decoded by IC8 (a one of 8 decoder) to produce a logical 1 on pin 12 and logical zeros on all other outputs. The logical 0 high level at pin 10 provides a logical 0 at pin 12 of IC12. This allows the first decade to run. The logical 0 at the output of IC12 pin 12 and the logical 0 from pin 11 of the IC8 produce a logical 1 state at pin 11 of IC11 which permits the second decade to count (these two decades require opposite preset signals). The logical 1 at pin 11 of IC11 provides a logical 0 at pin 8. The logical 1 from pin 12 of IC8 forces pin 3 of IC11 to go to the logical 0 state. This in turn presets IC5. The 0 state at this point provides a logical 0 at its output which presets IC4 to the count of 9. This action propagates down the chain presetting counters 3, 2 and 1 to the count of 9. Whenever IC6 reaches the count of 9, the buss connected to the base of transistor Q20 moves positive supplying the logical 0 to pin 11 of IC12. When IC7 reaches the count of 9, lines 9 and 10 go to a logical 0 state which provides a logical 0 from pin 8 of IC12. This output pulse, which is 1 clock cycle long, is supplied to the buss driving

amplifier, Q35 and Q36. Since we are in fact counting down, current switch transistor Q37 is turned on and transistor Q38 is turned off, as is transistor Q40. So the only amplifier on the buss is the one driven from the count down. This in turn supplies the signal for the output of the board via transistors Q45 and Q46 and to the external trigger amplifier, Q41, Q42, Q47, Q48, and Q49.

The board's output amplifier drives twin 93 ohm coaxial cables in a differential mode to supply drive to the input of the width and delay module. The trigger output amplifier which consists of two current mode amplifier stages and an emitter follower, Q49, is intended to drive a 50 ohm load. However, this circuit is series back matched and will drive any arbitrary external impedance. When a gating signal is to be applied to the internal clock, a positive level is supplied to the base of transistor Q19 via the protective diode bridge, CR1 through CR4. Q19 functions as a buffer stage to drive IC13 and IC14 which function to provide inversion of the input signal under the control of the gate ON OFF functional input. In the gate OFF mode, the output of IC13, pin 6, is at a logical 0 state. This condition allows the decade divider to operate and bias transistor Q21 ON while cutting off transistor Q22. In this condition the base of transistor Q6 will bias one diode drop positive with respect to the bias voltage of transistors Q2 and Q3, hence transistor Q4 will not conduct. When a positive signal is applied to the gate input, transistor Q21 is turned off, Q22 turns on, biasing Q4 to a voltage 1 diode drop negative with respect to the base of Q3. This in turn robs the emitter current from transistor Q3 and conducts it to ground via the collector of Q4. This disables the clock and places it in a condition ready to start the next cycle.

The applied gating signal also causes the preset counter (via a logical 1 at pin 2 of IC12) to preset the decade divider to a count of 899999 so that the first clock pulse will cause IC Q7 to produce an output signal and hence to produce the appropriate drive for the width and delay board in response to the removal of the gate OFF signal. Of course if the functional control line is in the gate ON mode, exactly the opposite operation occurs. That is, the clock is normally disabled and the counter is normally preset to 899999, and when a positive signal is applied to the gating input, the clock turns on and a count down goes into normal operation.

The external drive signal is applied to transistors Q31 and Q32 through the protective diode bridge CR25, CR26, CR27 and CR28 and coupling zener CR29A. These transistors form a Schmidt trigger that shapes the input signal and drives the buss amplifier, Q33 and Q34. In the external mode, current is supplied to the emitter of transistors Q33 and Q34 via transistor Q40 while transistors Q38 and Q37 are disabled.

c. Width and Delay Module. The input signal to the width and delay module is supplied to the bases of current mode gating stage Q22, Q23, and Q24 via zener diodes CR4 and CR5. When a gating signal is applied to the gate input, the flip-flop, which is made up of two of the gates of IC3, toggles on the clock pulse so as to provide a coherent gate signal to the gating transistor Q24. Q24 is biased to remove current from the emitters of Q22 and Q23 and disables the stage. When the input signal returns to ground, Q24 is returned to a normal high state and cuts off. The current is then rerouted to the current mode amplifier, Q22 and Q23. The output of this stage drives coaxial clipping lines to provide a narrow 5 nanosecond spike on each transition of

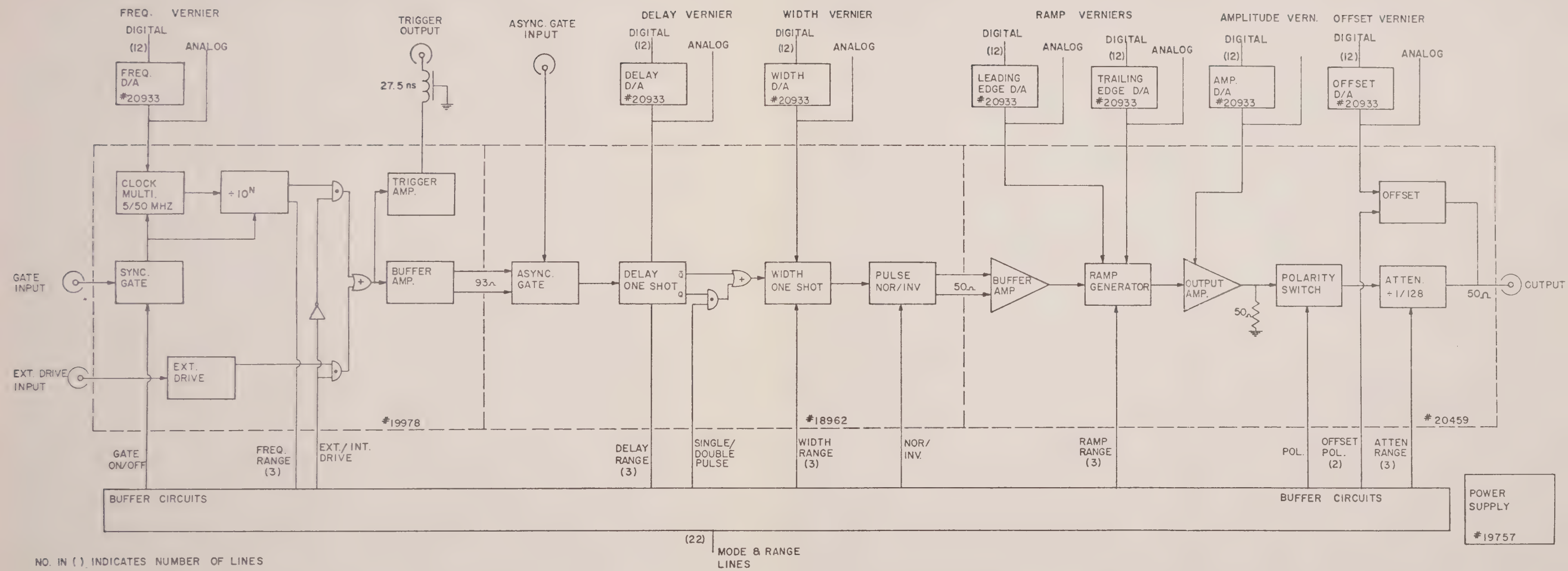


Figure 3-1 Block Diagram

the input signal. The positive pulse from transistor Q23 and the negative pulse from transistor Q22 are used to drive the delay one-shot. In order to maintain proper circuit and clipping line action the unused pulses from these collectors are terminated in resistors R74 and R75.

The delay one-shot consists of transistors Q25, Q26, and Q27 and their associated circuitry. This multivibrator operates in the following fashion. Normally transistors Q27 and Q26 are on and transistor Q25 is off. The collector potential of Q27 is determined by the negative clamp diode, CR3. When the gating amplifier provides a trigger pulse to the one-shot transistor, Q25 turns on and Q26 and Q27 are turned off. The collector potential of Q27 then rises to the positive clamp potential set by CR2.

The emitter of transistor Q26 is provided with a capacitance to ground and with a positive current source. This current source charges the emitter of this transistor in a positive direction until transistor Q26 begins to turn on. This action again turns transistor Q27 on and regeneratively drives transistor Q26 so that the timing capacitor in the emitter of Q26 is rapidly discharged through the base clamping diode CR13. Once the timing capacitor is recharged the one-shot is back in its normal rest condition ready to be triggered again.

The delay vernier control provides the reference voltage for positive clamp CR2 via the transistor buffer amplifier chain Q17, Q18, and Q19. Varying this bias voltage to the positive clamp diode determines the change in voltage of the timing capacitors and hence the period of the one-shot. Since we are programming the change in voltage to a capacitor, we are in effect directly controlling the period of the one-shot. The 8 ranges of this one-shot are provided by capacitors C8, C25, C26, C27, and C42 and by varying the charging current to the timing capacitors as supplied by the current source transistor, Q10.

The ranging circuit operates in the following manner. A range input is supplied to the 1 of 8 decoder, IC2, which in turn activates the transistor switches to turn on the appropriate timing capacitors and controls the current source for the timing capacitors. In the shortest delay range, none of the programmable timing capacitors are activated. Hence, C8 is the only timing capacitor in the circuit while transistor Q7 is saturated. Approximately 10 milliamps of charging current is available to the timing capacitor during this time. In the next lower range, 100 nanoseconds to 1 microsecond, pin 2 of IC2 goes to a logical 1 state which turns on transistors Q57 and Q55 and switching transistor Q56, which connects the timing capacitor, C27, to ground. On the next range down pin 2 goes to a logical 0 and pin 3 becomes a logical 1. This in turn saturates switching transistor Q42 which connects timing capacitor, C25, to ground. In the 10 microsecond to 100 microsecond range, the next range down, pin 4 becomes a logical 1 with all other pins at logical 0, which again activates switching transistor Q42, thus connecting capacitor C25 to ground and also supplies a logic 1 to the input of IC1 producing a logic 0 at the output pin 3 of IC1. This high logic level causes transistor Q7 to be cut off reducing the timing current by a factor of 10. Transistor Q28 is also cut off, reducing the bias current to the one-shot. This causes an approximate decade step in the time required to charge capacitor C25. The error term generated is due to the change in bias current to the timing transistor. This is corrected by the current supply to R137, and to the base of transistor Q20, the bias source for the negative clamp. The 100 microsecond to 1 millisecond range is generated when the

input causes pin 13 to become a logical 1. With this input low, timing capacitor C26 is activated, and the charging current is returned to 10 milliamps. In the 1 millisecond to 10 millisecond range, the logic 1 is on pin 12 of IC2, which reduces the charging current to the timing capacitor by a factor of 10 while maintaining capacitor C26 active in the circuit. On the 10ms–100ms range C42 is activated and the charging current is 10 milliamps. On the 100ms–1s range, the charging current is reduced by a factor of ten.

(1) Delay Buffer Amplifier. The output of the delay one-shot is coupled via NPN current mode pair Q29 and Q30 to the bases of the current mode pair, Q31 and Q32, whose collectors are differentiated in clipping lines CL3 and CL4 and provide the appropriate drive pulses for the OR gate.

The single pulse/double pulse OR gate always supplies drive pulses to the width one-shot via diodes CR23, CR24, CR38, CR39, and CR40. This pair of signals provides a drive pulse to the width one-shot at the end of each delay interval. In the double pulse mode, diodes CR31, CR32, CR35, CR36, and CR37 also supply pulses to the width one-shot. This OR gate is so designed and controlled that it always provides an approximate 91 ohm terminating resistor for the clipping lines. This provides a 5 ns wide pulse at the input of the OR gate under all operating conditions.

(2) Width One-Shot. The width one-shot consists of transistors Q33, Q34, Q35 and their associated circuitry. This circuit operates in exactly the same fashion as does the delay one-shot and will not be discussed in any further detail.

The output of the width one-shot drives current mode pair Q38 and Q39. As a function of the normal inverted control line (pin C7) either transistor Q36 or Q37 is saturated. The saturated transistor shorts the current mode pair collector to the +5 volt supply eliminating the output signal from this source. The other transistor is cut off and allows the signal from its collector to be coupled to the base of the output buffer Q40 and Q41. This signal is amplified by the buffer stage and drives a balanced 50 ohm transmission line system to the output board. When the normal/inverted line is placed in the opposite state, the opposite collector of the current mode pair, Q38 and Q39, is connected to the base of the output drive pair.

d. Type C Output Board. The input signal for the output board is applied through isolation transformer T1 to the dc restoring flip-flop, Q7 and Q8, through the differentiating capacitor, C1. This circuit is utilized to provide isolation of the output circuit from the timing circuits. The output of the restoring flip-flop drives a two stage current mode amplifier, Q50 and Q51, and Q18 and Q19. This amplifier in turn drives the current switching bridge which consists of transistors Q55 and Q56 for the current source side and transistors Q57 and Q58 for the current sink side. In the final analysis this entire circuitry simply determines whether current source Q11 and Q12 or current sink Q53 and Q54 are connected to the input side of R66. The output of this resistor, R66, provides either a constant current source or a constant current sink for the timing capacitors. The constant current charging and discharging of these timing capacitors provides the necessary linear ramps for the output amplifier section. The input of this amplifier is transistor Q27 which is an emitter follower which drives a current mode pair consisting of driver transistors Q28, Q59 and Q60 and output transistors Q37 and Q62. The input transistors are operated in parallel as are the two output transistors. The output of this amplifier is coupled via a polarity switching relay and a balun to the

input of a pi network attenuator system. The first section of the attenuator is a divide by two network which is either enabled or disabled by relay K2. The second section is a divide by four attenuator which is controlled by relay K3. The final section, a divide by 16 attenuator, is controlled by K4. The output of this attenuator section is coupled directly to the output of the instrument. Also connected to the output of the attenuator is the offset circuit which provides an offset current to the output which is independent of the setting of the attenuator. The output amplifier also drives a 65-ohm resistor and other miscellaneous networks whose cumulative effect is to provide a 50-ohm source impedance for the pulse generator. This source impedance, of course, is provided to minimize the effect of cable reflections and mismatched loads. To illustrate this operation a positive, normal pulse's path will be outlined. When the pulse starts transistor Q7 is turned off. This results in the current sink, Q54, and Q55, being connected via transistor Q58 to the timing capacitor which has been selected. Before the pulse had occurred diode CR30 had clamped the timing capacitor and the emitter follower's base to a potential slightly positive of the $-20V$ levels. This action completely cuts off the output pair, transistors Q62 and Q37. As the timing capacitor starts to discharge the voltage on the emitter of Q27 moves in a negative direction which allows current to be switched from the driver, transistors Q28, Q59, and Q60, to the output pair and hence on to the polarity control relay. This transfer of current to the output continues until the clamping diode, CR31, catches the bases of the output driver transistors. Shortly after this occurs clamping diode CR29 catches the ramp timing capacitor and also prevents it from continuing in a negative direction. It should be pointed out that the current from current source transistor Q83 in the emitter circuit of the output amplifier is always sufficient to provide some on current for the driver transistors. The output of this amplifier is now coupled through the polarity switch which then selects the direction of input to the balun so that the pulse will be inverted before going to the attenuator. At the end of the pulse the input restoring flip-flop changes state and causes a current source, Q11 and Q12, to be coupled to the timing capacitor instead of the current sink via transistor Q56. This current now charges the timing capacitor in a positive direction. As soon as the timing capacitor has moved sufficiently far so that the emitter follower again starts to draw current, the current in the output pair begins to reduce. This current reduces to zero before the clamping diode, CR30, clamps the positive charging of the timing capacitor. The circuit is now ready to produce the next output pulse when again the restoring flip-flop changes state. The ramp timing capacitors are selected via the three data bits supplied to pins A1, A2, and A3. These signals are coupled via isolating transistors Q68, Q70, and Q72, Q73, Q74 and Q75 to the input of a 1 of 1 of 10 decoder. The output of this decoder drives transistor switches to pull in the appropriate timing capacitors and or relay. For the fastest ramps no capacitors are pulled in. For the next range down capacitor C43 and C11 are energized via switching transistor Q79. This is accomplished by causing pin 2 of IC1 to go to -35 volts which, in turn, saturates the switching transistor. In the next range relay K5 is activated and none of the capacitor ranges are pulled in. Activating this relay permanently connects capacitor C9 and C10 to the ramp timing buss. On all the remaining ranges one of the transistor switches, Q76 – Q78, is activated which, in turn, also activates the relay and maintains this part of the path in conduction. Whenever a capacitor is not in use its potential is pulled to the -35 volt

level via the 1 megohm discharging resistor, R162. Since the output of this board is floating with respect to ground some means must be provided for coupling between the floating supply and the ground reference supply. The input of the timing capacitor range circuit is a basic example of how this is accomplished. If range 1 is activated, transistor Q70 is turned on which pulls a small current from the -35 volt supply and at the same time transistor Q71 is turned on. This supplies a small amount of current to the sensing resistor, R153, which in turn causes a current to be pulled from the VO supply via transistor Q45 to exactly balance the current necessary to couple the digital information to the range select circuitry.

(1) Amplitude Control. Transistor Q1 provides the constant current bias for the amplitude vernier control whose input emitter follower is transistor Q1. This emitter follower drives the grounded base stage, Q3, which provides a gain of 0.5 to the incoming signal voltage and produces the amplitude setting information referenced to the $+15V$ supply at the collector of Q3. Transistor Q15 is utilized to communicate the amplitude information to the floating output circuitry. This form of analog coupling provides good isolation between the two supplies since the voltage on the base of Q16 never approaches the potential of the base of Q15. Transistors Q16 and Q17 drive emitter follower Q20 to establish the amplitude level of the output circuit. The potential of the emitter Q20 is coupled to a unity gain power driver, Q21 and Q22, which supplies the clamp level for diodes CR29 and CR31, thus controlling the amplitude of the output pulse. The collector of transistor Q20 is coupled to the base network for the output current source driving transistor, Q82. This circuit varies the amount of current supplied to the output stage to minimize distortion and to aid in rising the output voltage transfer function. Also connected to the collector of Q3 are two current source transistors which drive the leading and trailing edge ramp time vernier inputs.

(2) Leading Edge Vernier. The basic circuitry in this vernier operates in exactly the same manner as the input circuitry and isolation circuitry of the amplitude control. This circuitry is made up of transistors Q46, Q89, Q48, and Q52. However, unlike the amplitude control, the output of Q52 directly controls the current sink, Q53 and Q54. The programmed value of this leading-edge ramp time produces several secondary effects in the circuitry. These effects are minimized and or corrected by sampling the level of sink current that is being supplied to the timing capacitors.

Compensation for the effects of varying the leading edge program is accomplished by the two current source transistors, Q13 and Q14, whose base signal is derived from the output of the leading edge vernier isolation amplifier. Q14 applies a small correction to the amplitude circuit which minimizes the effect of changing the discharge currents and the emitter follower currents in the output amplifier chain. Transistor Q13 provides an edge balance and corrects the trailing edge vernier control so there is little or no effect due to leading edge programming. The primary need for correction arises from the finite beta of the emitter follower and, hence, its change of base current with the change of emitter current.

(3) Vernier Trailing Edge Programming. The vernier trailing edge programming circuitry is essentially identical to the leading edge vernier except it is not necessary to provide any compensation networks for this function. The amplifier transistor chain consists of Q4, Q88, Q5, Q6, Q9, and Q10, whose collector is the output of the isolation amplifier and which drives Q11 and Q12, the trailing edge current source.

(4) Offset Circuitry. When a logic 1 is applied to one of the offset polarity inputs IC3 decodes the condition and turns either Q24 or Q25 off. For any condition in which both of the inputs are either a logic 1 or a logic 0, both Q24 and Q25 are left on. The output of these two transistors control saturated current switches, Q36 and Q39, which disable the offset amplifier when their associated transistor is conducting. The offset vernier control is coupled via Q31 to the base of Q33 which acts as a level shifting transistor. R94, the offset range control, in the emitter of Q33 provide the full scale adjustment for the offset circuitry. The collector of Q33 drives complementary emitter followers Q34 and Q35. These supply the appropriate signal to the current source, transistors Q41 and Q42, for the positive offset current. This offset current is coupled to the output via the inductor chain L14 and L15. When negative offset is programmed the signal from the collector of Q32 drives the emitter follower Q38 which again supplies the appropriate signal to the negative current source, transistors Q40 and Q43. These transistors supply the negative offset current for the output.

f. Power Supply. The E-H Model 1501 Model 1501A utilizes four nearly identical power supplies to supply the analog circuitry and a fifth supply is utilized to deliver the voltage necessary for the logic circuitry. This supply utilizes a fixed reference IC (IC301 which is located on the chassis) and an over voltage and reverse polarity protection circuit which consists of CR1 and CR2, and CR3. The IC regulator is so designed that it automatically protects itself against short circuits. However, if an over-voltage condition exists the SCR CR2 is turned on via zener diode CR1 and its gate circuit, and effectively crow bars the power supply to ground. If for any reason the supply is shorted to the -15 V supply, diode CR3 clamps the supply to -0.7 V. In either case the digital ICs within the instrument are protected.

The remaining power supplies are similar to the +15 V supply which consists of IC1, Q304, and the associated circuitry. The output voltage of this supply is sensed by input pin 6 of IC1 at the junction of the voltage divider made up of R1 and the parallel combination of R6 and R7. The magnitude of the voltage at pin 6 with respect to ground is approximately 4 volts. This input produces a controlled signal at pin 3 of the IC which drives the base of the series pass transistor, Q304, whose emitter supplies the current for the +15 V supply. Before this current is passed to the supply buss, however, its magnitude is monitored via resistor R8. If the current through this resistor exceeds about 1-1/2 amps, pin 5 of the IC is moved in a negative direction which cuts off the output of IC1 turning off the series pass transistor and limiting the overall current of the supply. A secondary protection loop exists utilizing the internal current sensing capability of this IC via the feed back to pin 4. If the base current of Q304 exceeds 100 mA again, IC1 current limits and shuts down the supply. This supply is set within 1% of its nominal value at the factory and should remain within 1%.

g. Parallel D/A Converter. The operation of this D/A converter is conventional. A negative true input is applied to ICs 1 through 3. The output of these ICs control the transistor switches, Q2 through Q13, which directly program the weighted resistor network. The weighted resistor network, R4 through R15, provides a 1248 BCD coded input to the summing junction for operational amplifier IC1. If a 000 count is programmed none of the transistors are turned on and there is no current flowing through any of the resistors. As a result the current through resistors R40 and R41 is balanced against the current flowing in R45. The current in R45 is proportional to the voltage difference between the output of the operational amplifier and the inverting input. The voltage of the inverting input will be exactly the same as the voltage of the non-inverting input when the system reached equilibrium. Thus, if a proper current is supplied via R40 the output voltage of the operational amplifier will have to be exactly 0 volts when none of the resistors in the weighted ladder network are activated. When a resistor is connected to ground via the switching transistor, it reduces the total amount of current flowing towards the negative input of the operational amplifier and hence causes less current to flow through R45. This means the output voltage of IC1 must raise to exactly compensate for the resistor which has been connected to ground. The output voltage from the card is directly proportional to the digital input control. Range line buffering is provided by IC's 5-8.

SECTION 4

MAINTENANCE

4-1 GENERAL INFORMATION

This section of the manual gives maintenance notes and alignment procedures for the E-H Model 1501A. The instrument requires a minimum amount of maintenance; however, normal aging of electronic components may eventually cause abnormal operation. Use of the following procedures should forestall many minor malfunctions, or permit their detection before a major repair is required.

4-2 PREVENTIVE MAINTENANCE

a. Cleaning and Visual Inspection. A regular program of inspection and maintenance is recommended to minimize down-time. The operating environment and amount of usage will dictate how often the instrument should be cleaned; in the absence of more stringent conditions, inspection every four to six months is recommended. Check the instrument in the following manner:

(1) Disconnect the power cord. Inspect the exterior of the instrument for broken knobs, switches, or connectors.

(2) Remove the top and bottom covers using the disassembly procedure in Subsection 4-4. If the internal surfaces and components have an excessive amount of dust deposited on them, use a low-pressure stream of air and a soft brush to remove the foreign material.

CAUTION

Do not clean the printed circuit boards with solvents, since damage to the circuits may result.

(3) Check the physical integrity of components and wiring. Look for evidence of loose connections, broken terminals, leakage of insulation compounds, and heat damage. In most cases, the source of a visually detected trouble is easily located. In the case of heat damage however, care should be taken to locate the original cause of the overheating before the instrument is put back in service.

4-3 PERFORMANCE VERIFICATION PROCEDURE

The following procedure serves as a check of the Model 1501A's functional performance and its specifications. This procedure should be used when a malfunction is suspected, or as a part of routine maintenance.

NOTE

This procedure assumes front-panel controls are used. Such controls are optional

a. Recommended Test Equipment. The following is a list of the test equipment required for verifying operation and for calibration.

(1) Universal counter-timer capable of measuring frequency to 50 MHz and period to two seconds. Fluke Model 1952A or equivalent.

(2) Digital Voltmeter capable of measuring DC voltages to ± 35 V with better than 0.1% accuracy and 10 mV resolution. Fluke Model 8000A or equivalent.

(3) Sampling Oscilloscope, 350 ps risetime, digital readout, time accuracy $\pm 1\%$, voltage accuracy $\pm 2\%$, sweep speed 0.2 ns/div to 100 μ s/div, sensitivity 100 mV/div minimum. AMC Model 1100 or equivalent.

(4) Coaxial Attenuator, 50 ohms input/output, x2 attenuation. Tektronix 017-0080-00.

(5) Coaxial Attenuator, 50 ohms input/output, x10 attenuation. Tektronix 017-0078-00.

(6) Coaxial Termination, 50 ohms. E-H part number 693-41520 (mates with AMC 1100 remote sampling probe) or equivalent.

(7) Coaxial Termination, 50 ohms, Tektronix 011-0049-01.

(8) Coaxial Cable, RG-213/U or equivalent.

(9) Male BNC to GR874 adapter, Tektronix 017-0064-00 or equivalent.

(10) Pulse Generator, E-H Model G710 or equivalent.

(11) Adapter, BNC female to dual banana plug, Tektronix 103-0040-00.

b. Frequency Range Verification. This procedure checks the operating range of the internal clock.

(1) Set all front-panel PROGRAM MODE switches to the LOCAL position.

(2) Set front-panel switches as follows:

CLOCK	.	.	.	.	.	.	.	INT
GATE	.	.	.	.	.	.	.	OFF
PULSE MODE	.	.	.	.	.	.	.	SINGLE
WIDTH	.	.	.	.	.	.	.	10 ns
DELAY	.	.	.	.	.	.	.	10 ns
RAMPS	.	.	.	.	.	.	.	999 x3 V/ns

AMPLITUDE					
POLARITY	.	.	.	.	N+
RANGE	.	.	.	.	5.0 V
% OF RANGE	.	.	.	.	50.00
OFFSET	.	.	.	.	OFF

(3) Connect Model 1501A trigger output to input of Universal Counter-Timer. Set Counter-Timer for frequency measurement.

(4) Measure the Model 1501A output frequency at several points on each range. The frequency should be within $\pm 5\%$ of the setting. At low frequencies, the period mode of the Counter-Timer should be used for best resolution.

c. Width and Delay Verification. This procedure checks the operation and calibration accuracy of the pulse width and pulse delay circuits.

(1) If a sampling oscilloscope with internal triggering is available, connect the trigger output of the Model 1501A to one channel of the oscilloscope and the main pulse output to the other channel. Connect the two coaxial attenuators in series with the sampling oscilloscope input to prevent damage to the oscilloscope. If the AMC Model 1100 is used, connect the pulse output to the oscilloscope input and the trigger output to the oscilloscope trigger input.

(2) Procedure using internally triggered oscilloscope. Trigger oscilloscope on pulse generator trigger output trace. Measure the delay between the leading edge of the trigger waveform and the leading edge of the main pulse. The delay measured should be within $\pm 5\%$ of the setting, except on the 10 ms-100 ms and 100 ms-1 s ranges, where the accuracy is $\pm 15\%$. It may be necessary to use the time interval mode of the counter-timer to measure long delays. When using a sampling oscilloscope, the measurement error due to the oscilloscope must be taken into account when measuring time.

(3) Procedure using AMC 1100. Set PULSE MODE TO DOUBLE. Adjust delay control of Model 1100 to display trailing edge of first pulse and the entire second pulse. The pulse width may have to be adjusted to display the trailing edge of the first pulse. Set the Model 1100 to measure the time interval between the 50% points of the trailing edges of the two pulses. Measure the time interval at points on each range by setting the DELAY control. The interval measured should be within $\pm 5\%$ of the setting, except on the 10 ms-100 ms and 100 ms-1 s ranges, where the accuracy is $\pm 15\%$. It will be necessary to use the counter-timer as indicated above on the longer delay ranges.

NOTE

It will be necessary to change the pulse frequency as the delay setting is increased. Use a frequency that will give approximately 50% duty cycle.

(4) Trigger sampling oscilloscope externally from Model 1501A trigger output. Set delay control and oscilloscope sweep time to display the entire pulse. Measure the pulse width between the 50% points on the leading and trailing edges. It should be within $\pm 5\%$ of the setting, except on the 10 ms-100 ms and 100 ms-1 s ranges, where the accuracy is $\pm 15\%$. It will be necessary to use the counter-timer to measure the width. Keep delay and width within approximately 50% of the period, as noted above.

d. Amplitude and Offset Verification. This procedure checks the operation of the amplitude and offset circuits.

(1) Set Model 1501A controls as follows:

FREQUENCY	.	.	.	.	50 kHz
DELAY	.	.	.	.	as required
WIDTH	.	.	.	.	50 ns
RAMPS	.	.	.	.	999 x 3 V/ns
PULSE MODE	.	.	.	.	SINGLE
OFFSET	.	.	.	.	OFF, 0000 V
AMPLITUDE					
RANGE	.	.	.	.	10.0 V
% OF RANGE	.	.	.	.	99.95

All other controls should be left in the positions specified in step b(2) above.

(2) Connect the Model 1501A pulse output (through the two coaxial attenuators in series) to the sampling oscilloscope input. Connect the trigger output to the trigger input of the oscilloscope. Trigger the oscilloscope and adjust the DELAY control so that the pulse waveform appears on the screen.

(3) Measure the peak-to-peak pulse amplitude (excluding any overshoot or ringing). It should be 10 V $\pm 5\%$.

(4) Check the programmed amplitude at other points on the 10.0 V range. It should be within the tolerance specified.

(5) Set the RANGE switch to the other positions. The amplitude should decrease by a factor of two on each range.

(6) Set the GATE switch to the ON position. This disables the pulse output. Connect the output of the Model 1501A to the input of the digital voltmeter, using a 50 ohm termination at the digital voltmeter input.

(7) Set the OFFSET switch to POS and measure the offset voltage at several points over the range. The voltage measured should be within $\pm 5\%$ of the setting.

(8) Set the OFFSET switch to NEG and repeat step (7) above.

e. Rise and Fall Time Verification. This procedure checks the range and programming accuracy of the rise and fall ramps.

(1) Connect the output of the Model 1501A to the input of the sampling oscilloscope. Connect the two coaxial attenuators in series with the sampling oscilloscope input. Connect the trigger output to the oscilloscope trigger input.

(2) Set Model 1501A controls as follows:

FREQUENCY	.	.	.	.	50 kHz
WIDTH	.	.	.	.	50 ns
DELAY	.	.	.	.	20 ns
AMPLITUDE					
POLARITY	.	.	.	.	N+
RANGE	.	.	.	.	10.0 V
% OF RANGE	.	.	.	.	99.95
OFFSET	.	.	.	.	OFF
GATE	.	.	.	.	OFF

Other controls should be left as in step b(2) above.

(3) Set RAMPS switch to .999 x3 V/ns. Measure 10-90% rise and fall times. WIDTH and DELAY switches may have to be adjusted to center the waveform on the screen and give a flat top on the pulse. The rise and fall times should be less than 3 ns.

(4) Set RAMPS RISE AND FALL switches to .999 V/ns. The rise and fall times should be 10.0 ns $\pm 5\%$ ± 3 ns. Check other points within the range; the rise and fall times should be within the tolerance specified. It will be necessary to adjust width, delay and oscilloscope sweep to make the required measurement.

(5) Check all rise and fall ranges as in step (4) above.

f. Miscellaneous Function Verification. This procedure checks the external drive, gating, pulse polarity, and pulse inversion functions.

(1) Connect the pulse generator to Model 1501A external drive input connector J105. Adjust pulse generator output amplitude to approximately +1.5 V.

(2) Set Model 1501A CLOCK switch to EXT position. Observe Model 1501A output and vary pulse generator frequency. The Model 1501A frequency should follow the pulse generator frequency.

(3) Set POLARITY to N-. The pulse should now be negative-going with the same baseline.

(4) Set POLARITY to I+. The pulse should now be inverted, with the pulsetop at the baseline and vice versa.

(5) Set CLOCK to INT. Connect pulse generator output to Model 1501A synchronous gate input connector J107. Monitor the main pulse output as well as the trigger output.

(6) Set GATE to ON. Adjust pulse generator output until amplitude exceeds +1.5 V. The Model 1501A output should be gated on for the duration of the gating signal and the trigger output should also be gated.

(7) Set GATE to OFF. The Model 1501A main output and trigger output should be gated off during the gate pulse.

(8) Connect pulse generator output to asynchronous gate input connector J106. Monitor main pulse output and trigger output.

(9) In both gate on and gate off operation, the main pulse output should be gated, but the trigger output should run continuously. This completes performance verification.

4-4 RECALIBRATION PROCEDURE

a. General. The recalibration procedure should be performed only when components are replaced or when the instrument fails to meet specifications. Recalibration should not be performed on a routine basis.

b. Recommended Test Equipment. The test equipment required for recalibration is the same as that required for performance verification.

c. Procedure.

WARNING

WHEN TOP AND BOTTOM COVERS ARE REMOVED, HAZARDOUS VOLTAGES ARE EXPOSED WHEN PRIMARY POWER IS CONNECTED. USE CAUTION WHEN WORKING NEAR THE POWER TRANSFORMER OR AC POWER INPUT.

(1) Turn Model 1501A off and disconnect primary power. Remove top and bottom covers.

(2) Set Model 1501A on its bottom and reconnect primary power. Turn instrument on and allow a 10-15 minute warmup period.

(3) Connect the digital voltmeter between ground test point and +15 V test point. Check that the voltage is +15 V ± 150 mV.

(4) Connect the digital voltmeter high side probe to -15 V test point. Check that the voltage is -15 V ± 150 mV. If either voltage is out of tolerance, R7 in the +15 V supply must be padded with resistors in parallel. The resistors used to pad R7 and R13 should be 1% metal film type.

(5) Connect the digital voltmeter high side probe to the +5 V test point. The voltage should be +5 V ± 0.5 V.

(6) Connect the digital voltmeter between ground test point and frequency test point. Set FREQUENCY vernier to 0000 (range unimportant) and adjust R27 on the frequency D/A converter board for a reading of less than 1 mV on the digital voltmeter.

(7) Set FREQUENCY vernier to maximum count and adjust R30 on the frequency D/A board for a reading of 4.995 V ± 10 mV.

(8) Repeat steps (6) and (7) until no further adjustment is necessary.

(9) Repeat procedures for delay, width, leading, trailing, amplitude, and offset D/A converters. Use 000 and maximum count settings, except for front panel control of amplitude D/A where a minimum count of 5000=0 ± 1 mV.

(10) Set FREQUENCY to 25.0 MHz. Connect trigger output to input of frequency counter. Set delay and width to 10 ns. Other control settings should be as follows:

CLOCK	.	.	.	.	.	.	INT
GATE	.	.	.	.	.	.	OFF
PULSE MODE	.	.	.	.	.	.	SINGLE
OFFSET	.	.	.	.	.	.	OFF
AMPLITUDE	Positive Normal 2.5 V, Amp.						

(11) Adjust R68 on the clock board for a frequency reading of 25.0 MHz $\pm 2\%$.

(12) Set FREQUENCY to 49.95 MHz. Adjust R53 on the clock board for a reading of 49.95 MHz $\pm 2\%$.

(13) Set FREQUENCY to 5.00 MHz. Adjust R26 on the clock board for a reading of 5.00 MHz $\pm 2\%$.

(14) Repeat steps 10-13 until low, middle and high frequencies fall within the required tolerance.

NOTE

It may be possible to calibrate the clock frequency to better than the specified $\pm 2\%$. It is to the advantage of the user to calibrate the instrument as closely as possible. The 5-50 MHz range is controlled by analog circuits; the other ranges are divided digitally from this range. It should be noted that the $\pm 1\%$ repeatability is a function of the D/A circuit and cannot be improved.

(15) Turn off primary power and mount the width and delay board on an extender. Turn on primary power.

(16) Connect the output of the Model 1501A to the input of the digital readout oscilloscope. Connect the Model 1501A trigger output to the oscilloscope trigger input.

(17) Set controls as follows:

DELAY 50 ns
FREQUENCY 50 kHz

All other controls should be left as specified in step (10) above.

(18) Set WIDTH to 1 μ s. Adjust R60 on the width and delay board for a pulse width of 1 μ s $\pm 2\%$.

(19) Set WIDTH to 9.99 μ s. Adjust R46 for a pulse width of 9.99 μ s $\pm 2\%$.

(20) Set WIDTH to 99.9 ns and frequency to 49.95 kHz. Adjust R185 for a reading between 95 and 108 ns.

(21) Repeat steps 18, 19 and 20 until no further adjustment is necessary.

NOTE

In the above steps, and following steps, it is desirable to calibrate to better than $\pm 2\%$ if possible, to allow for temperature drift and aging of components.

(22) Set Width to 10.0 μ s and frequency to 5 kHz. Adjust R179 for best accuracy.

(23) Set WIDTH to 99.9 μ s. Adjust R52 for best accuracy.

(24) Repeat adjustments until no further interaction is observed.

(25) Reduce frequency to 1 kHz and set WIDTH to 5.00 ms. Observe width reading. If error is greater than specified, readjust R52 and R179 until reading is within tolerance.

(26) Check steps 18 to 20 to be sure that the 1-10 μ s range is still within tolerance required.

(27) Repeat adjustments until no further interaction is observed.

(28) Set PULSE MODE to DOUBLE and WIDTH to 10.0 ns.

(29) Repeat steps 18-27 for the delay circuit, using the DELAY control wherever WIDTH is specified, and measuring the delay from the 50% point on the trailing edge of the first pulse to the 50% point on the trailing edge of the second pulse. The adjustments for delay are as follows:

Step 18 - R17
Step 19 - R21
Step 20 - R138
Step 22 - R136
Step 23 - R26
Step 25 - R26, R136

(30) The next steps in the procedure calibrate the pulse amplitude, and require that two of the power supplies on the power supply board be adjusted using adjustments found on the output board. The voltages are measured with respect to the floating ground on the output board (not chassis ground). Floating ground is on pins B-T and B-16, -20 V is on A-S and A-15, and -35 V is on pins A-R and A-14. Adjust R201 to adjust the -20 V supply to -20 V ± 100 mV. Adjust R204 to bring the -35 V supply to -35 V ± 100 mV.

(31) Set controls as follows:

PULSE MODE SINGLE
FREQUENCY 10 kHz
DELAY 20 ns
WIDTH 100 ns
AMPLITUDE Positive Normal,
x1 Attenuation and 5
volt Amplitude

(32) Measure the voltage across R20 on the output board. Record this voltage.

(33) Set amplitude vernier to maximum count. Adjust R7 on the output board until the voltage reading is *exactly* twice the value measured and recorded in step 32.

(34) Invert pulse and set amplitude for 5 V. Adjust R65 for an output pulse amplitude to 5.08 V to 5.13 V.

(35) Set amplitude vernier to maximum count. Adjust R55 for a pulse amplitude of from 10.2 to 10.3 V.

(36) Repeat steps 34 and 35 until both voltages are within the specified ranges.

(37) The following steps calibrate the offset circuits. First, replace R175 on the output board with a 5.1 k Ω , 1% metal film resistor. Then temporarily replace R121 with a 10 k Ω potentiometer. (The potentiometer will be replaced with a fixed-value 1% metal film resistor later.)

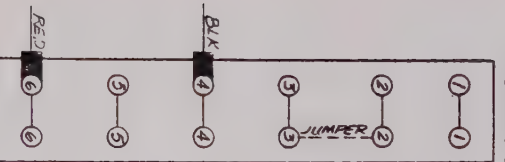
(38) Program the 1501A for Positive Normal output on the 10 volt (Attenuation Range 7) range, for 5 volts output. Terminate output with a 50 Ω resistor. Set the clock to EXT. DRIVE.

(39) Program OFFSET for +50mV. Adjust the zero adjust potentiometer on the D/A converter board until the output is +50mV ± 5 mV.

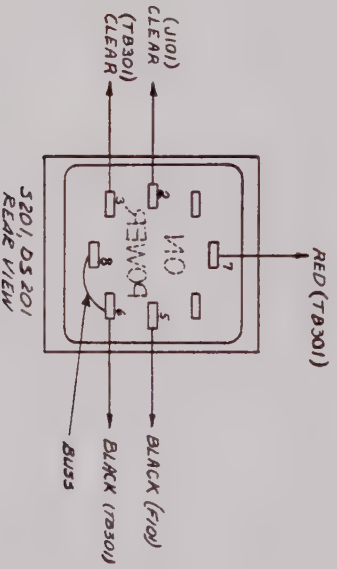
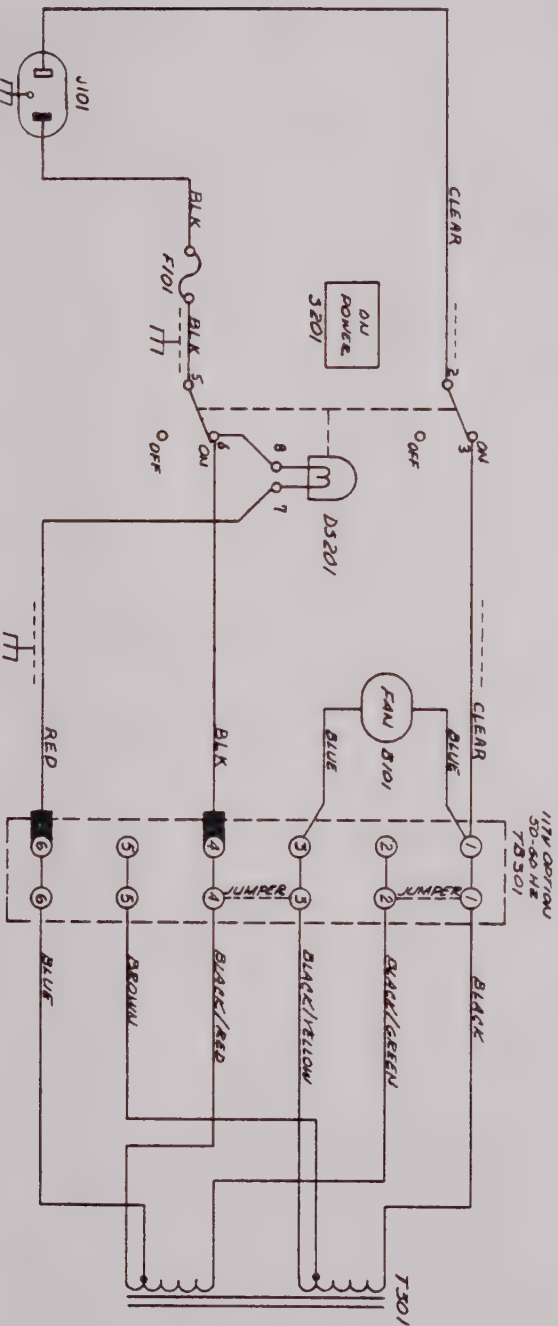
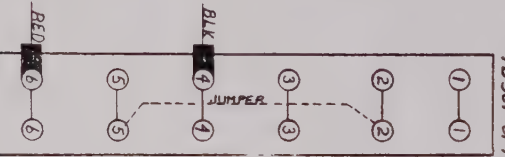
100V 50-60Hz
7B301 OPTION



250V 50-60Hz
7B301 OPTION

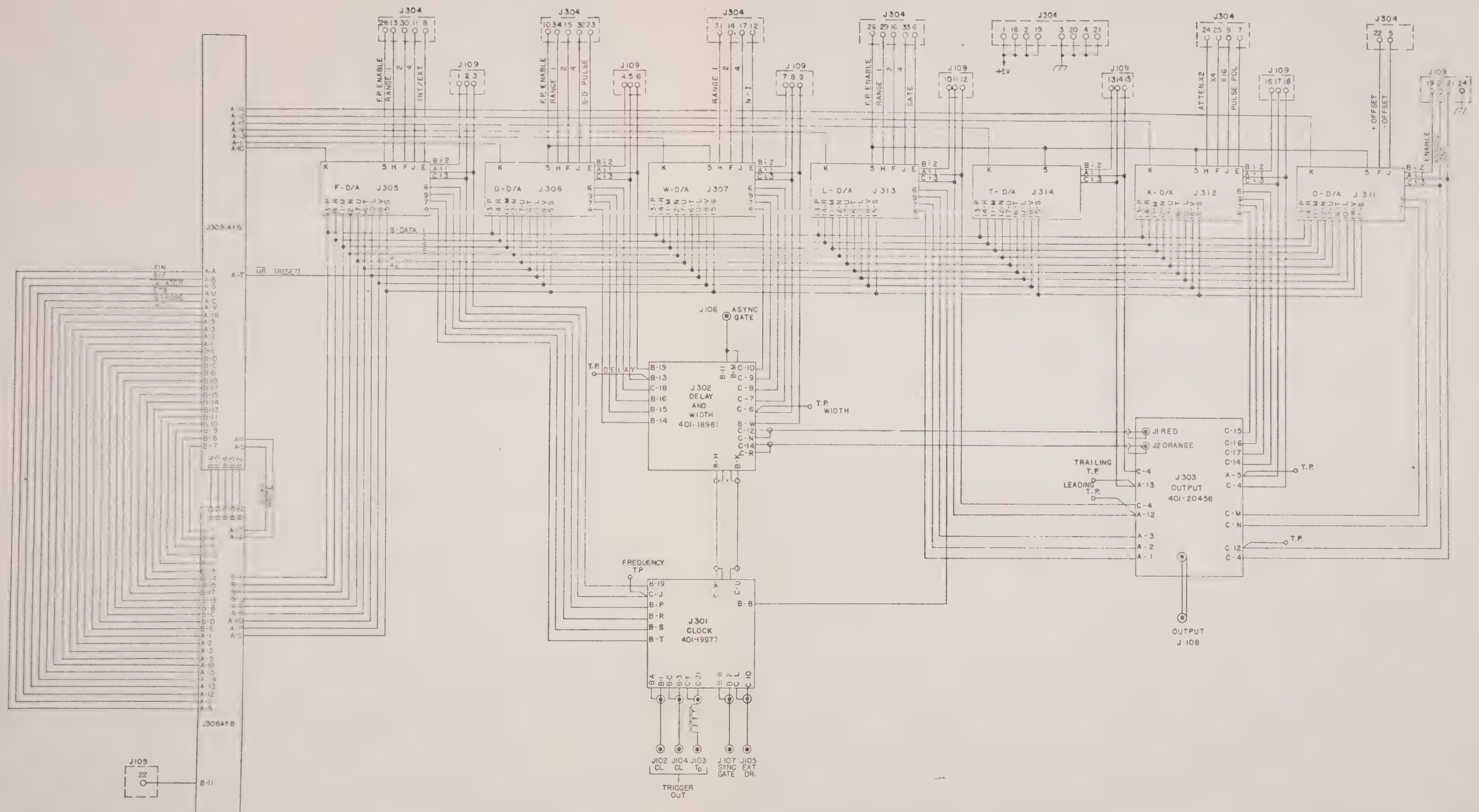


217V 50-60 Hz
7B301 OPTION



5201 DS201
REAR VIEW

STANDARD,
WIRING AC
PRIMARY SIDE OF T 501



MASTER
SCHEMATIC
(NEUTER)

1501 A
140-
F21232 B

(40) Program OFFSET for +5V. Adjust the offset range potentiometer R94 on the output board for an output of +5V ± 50 mV.

(41) Program OFFSET for -5V. Adjust the negative offset potentiometer R104 on the output board for an output of -5V ± 50 mV.

(42) Program OFFSET for -50 mV. Adjust the 10 k Ω potentiometer installed in step 37 for an output of -50 mV ± 5 mV. Remove the 10 k Ω potentiometer and measure its resistance. Replace it with a 1% metal film fixed-value resistor of equivalent $\pm 1\%$.

(43) Recheck outputs with OFFSET programmed for +50 mV, -50 mV, +5 V, and -5 V. Readjust controls if all values are not within specified tolerances.

(44) The following steps calibrate the leading and trailing edge ramps. All measurements are made between the 10% and 90% points. In all cases, a pulse width and repetition frequency consistent with the leading and trailing edge time must be maintained. Also, an oscilloscope sweep time consistent with the time being measured should be maintained. Although the programming accuracy is stated as $\pm 5\%$, calibration should be made as accurately as possible to ensure that the instrument will meet specifications after taking into account temperature variation and component aging.

(45) Set controls as follows:

```

FREQUENCY ..... 6 kHz
WIDTH ..... 30  $\mu$ s
DELAY ..... 25 ns
AMPLITUDE ..... Positive normal
                               10 V Amplitude
OFFSET ..... .000
CLOCK ..... INT
GATE ON ..... FALSE
PULSE MODE ..... SINGLE
  
```

(46) Set ramp range to 10 V/ μ sec-1 V/ μ sec range; leading and trailing edge verniers to 100. Adjust R34 on the output board for a leading edge time of 8 μ s $\pm \%$.

(47) Set leading edge vernier to maximum count. Adjust R71 for a time of 0.8 μ s.

(48) Repeat steps 46 and 47 until both time measurements are within specified ranges.

(49) Set AMPLITUDE to Positive Inverted and TRAILING EDGE vernier to 100. Adjust R25 for a time of 8 μ s.

(50) Alternately set the LEADING EDGE vernier at 10% of range and full scale and adjust R57 until the change no longer affects the trailing edge.

(51) Set TRAILING EDGE vernier to maximum count and adjust R31 for a reading of 0.8 μ s.

(52) Set TRAILING EDGE vernier to 100 and adjust R25 for a reading of 8 μ s.

(53) Repeat steps 51 and 52 until both time measurements are within specified ranges.

(54) Return the 1501A to a positive normal pulse.

(55) Set both leading and trailing edges to 500 V/ μ sec. Adjust C43 (using an insulated screwdriver) so that both leading and trailing edges have the same measured value. This completes the calibration procedure.

4-5 TROUBLE-SHOOTING PROCEDURE

a. General. The information presented in this section is for the expressed purpose of simplifying and speeding the isolation of any fault that may occur within the instrument. Before attempting to do any major maintenance on this instrument the following test equipment should be available.

- (1) A digital voltmeter capable of making measurements to an absolute accuracy of less than 0.1%.
- (2) A sampling scope with less than 350 p sec. rise time.
- (3) Some method of parallel programming the instrument in digital form.
- (4) A pulse stimulus to drive the external gate, external drive and asynchronous gate inputs.

b. Preliminary Step. Before attempting any other maintenance on the instrument the power supply voltages should be checked to determine that they are within their specified accuracies of: +15 ± 0.15 V, -15 ± 0.15 V, +5 ± 0.5 V as measured on the test points on the chassis with a power supply voltage between the nominally specified limits. The output of the D/A converters should also be checked, first with a count of 800 on each of the D/A cards thus providing an output voltage of 0 ± 5 mV. Assuming these conditions are met, the following outline should help isolate the trouble.

c. No Trigger Output Pulse. For any clock vernier or range setting, if the instrument operates normally in every other respect, the problem is in the trigger output amplifier and transistors Q41, Q42, Q47, Q48, and Q49 should be checked. If there is also no output pulse the problem is in either the clock circuit, Q4 and Q5, and their associated current sources and circuitry, or in the clock buffer amplifier, Q9 and Q10, or Q29 and Q30. A 5K sampling probe should be used to measure the waveform on the collector of Q4. This should be a square wave of approximately 1 V amplitude at the programmed frequency. If the square wave is present the signal should be followed to the amplifier chain until the fault is detected. If it is not present it is necessary to trouble-shoot the circuitry associated with these two transistors.

d. Clock Operates Correctly Only on Range 7. Program range 6 and measure the signal on pin 8 of IC7. This should be a signal of at least 1.5 V amplitude whose base line is less than 0.5 V from ground. If the signal is not present transistor Q14, Q15, and Q18 or their associated circuitry has malfunctioned. If the signal is present check pin 1 for a low measurement. If 1 is not low then either IC12 or IC8 has malfunctioned. If it is low, check pin 8 of IC12 for a pulse whose duty cycle is 20% and whose repetition frequency is 1/10 that of the basic clock frequency. If the signal is present transistor Q35 or Q36 has failed. If the signal is not present and pin 11 is in the high state, IC12 or IC7 has failed. If pin 11 is in the low state check Q20's base which should be at

approximately +5 V. If it is not at +5 V one of the divider chain, IC1 through IC6, has failed to preset and this can be determined by checking the voltage at pins 12 and 11 of these ICs. The levels should all be greater than +2 V.

e. Clock Stops On Lower Ranges. This indicates that the divider network is not operating properly. Check to determine that the appropriate logic 1 is presented at the output of IC8 in all cases. If this does not define the problem, program in range 0 and determine that each of the decade counters is operating normally. This should isolate the problem.

f. Some Delay Ranges Missing. Check to determine that the output of IC2 produces a logical 1 on the range that is missing. If not, IC2 is defective. If it does, determine that the transistor associated with the timing capacitor on that range is in fact saturated for the range. If not, the problem is in the chain between the output of the MC4006 and the timing capacitor's switching transistor.

g. Some Width Ranges Missing. If the output of IC5 is producing a logical 1 on the desired range the problem is in the range switch transistor or its associated drive chain.

h. Width or Delay Ranges 3 and 5 Too Short. For the delay IC1 is defective or transistor Q7 or Q44 is defective. For the width circuit IC6 is defective or transistor Q16 or Q49 is defective.

i. No Output Pulse From Width Or Delay Board. The following is a quick procedure to localize the problem. Determine that the clock pulse appears on connector B of the width and delay card, pins 7 and 9. These two pulses should be reciprocals of each other. If the pulse is there the clock is operating correctly and the coaxial connections are satisfactory. Check the collector of Q30 to determine that the delay one-shot is programming correctly. Use a 5 K sampling probe. If no pulse appears here the delay one-shot has malfunctioned. Check the base of Q38 to determine that the width one-shot is operating correctly. No pulse at this point indicates that the width one-shot has malfunctioned. With an output board connected determine that there are drive pulses at pins C12 and C14 of the width and delay card. These pulses will be differentiated by the output board and will have an exponential character. If no pulses are present one of the following four transistors is bad or the normal inverted control circuitry has failed. Q38, Q39, Q40, and Q41 should be checked along with their associated circuitry.

j. No Output Pulse. First, determine the width drive pulse applied to J1 and J2 is present on both connectors. Next measure the voltage across C34 and if necessary adjust

R201 to produce a $-20\text{ V} \pm 0.1\text{ V}$ for this supply. Next measure the voltage across C35 and adjust, if necessary, R204 to produce a $-15 \pm 0.15\text{ V}$ to this supply. If either or both of these power supplies will not adjust properly check the associated regulator on the power supply card. Next determine whether there is a negative output pulse present on the collector of the output transistors, Q62 and Q37. If this pulse is present the trouble is probably a bad balun connection or a defective relay. If the pulse is not present, observe the emitter of transistor Q27 which should be setting at approximately -19.5 V and should be producing a negative going pulse of at least 1.5 V amplitude. This test point is easily recognized as it is the triangular shaped piece mounted above the back of the board in the middle of the assembly. If this pulse is present the problem is either in the driver or in the output transistors, the 11780's, or possibly in their current source, transistor Q83. If a pulse is present at this point, but its level is wrong, check the clamping diodes, CR29, CR30, and CR31. If no pulse appears check the base of transistor Q55 and determine that a reasonable drive pulse is present. If there is a pulse at the base of Q55, approximately 1 V amplitude, the drive amplifier is operating properly. If not, the circuit must be trouble-shot from stage to stage. If there is a pulse present at this point and there is still no output pulse the level on the base of transistor Q27 will indicate whether the current source or the current sink is at fault and the circuitry is checked in a similar manner.

k. Calibration. If any extensive repairs are necessary to any of the modules of this instrument, that module alone should be completely recalibrated following the calibration procedure in this manual. It is not necessary to calibrate the D/A cards when repairs have been made to the functional boards and conversely when D/A cards have malfunctioned and have been replaced or repaired there is no need to recalibrate the functional module if the D/A cards are calibrated according to the procedure included in this manual.

4-6. RECOMMENDED SPARE PARTS

Table 4-1 lists the recommended spare parts required for maintenance of the Model 1501A. The first part of the list is a list of the major assemblies that may be purchased as spares by those who do not intend to repair subassemblies or components. The second part includes active electronic components and high- failure items such as relays and fuses.

See Section 5 for a complete list of all parts of the Model 1501A.

RECOMMENDED SPARE PARTS LIST

MODEL 1501ADATE April 1975

PART NUMBER	DESCRIPTION	QUANTITY USED	RECOM- MENDED SPARES	PRICE
	Printed Circuit Boards			
401-19756	Power Supply Regulator Assy	1	1	
401-19977	Type B Clock Assy	1	1	
401-22373	Delay & Width Assy	1	1	
401-20458	Type C Output Assy	1	1	
401-21212	Parallel D/A Converter Assy	7	2	

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Table 4-1 Recommended Spare Parts List (1 of 3)

RECOMMENDED SPARE PARTS LIST

MODEL 1501ADATE April 1975

PART NUMBER	DESCRIPTION	QUANTITY USED	RECOM- MENDED SPARES	PRICE
Zener Diodes				
374-00022	1N751A	1	1	
00037	1N759A	1	1	
00044	1N749A	1	1	
00080	1N747A	1	1	
11733	E-H Selected	1	1	
11761	E-H Selected	1	1	
11797	E-H Selected	1	1	
12529	E-H Selected	1	1	
Diodes				
376-00022	1N914B	39	4	
00031	1N270	4	1	
00700	MBD101	23	4	
11764	E-H Selected	10	2	
22925	E-H Selected	3	1	
Misc. Parts				
396-00001	Fuse Holder	1	1	
398-00002	Fuse 2 Amp S.B.	1	1	
510-00020	Power Light	1	1	
584-00018	Relay Zestron 226-12-1A	1	1	
584-00019	Relay Hi G	4	1	

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Table 4-1 Recommended Spare Parts List (2 of 3)

RECOMMENDED SPARE PARTS LIST

MODEL 1501ADATE April 1975

PART NUMBER	DESCRIPTION	QUANTITY USED	RECOMMENDED SPARES	PRICE
Transistors				
663-00070	2N3904	165	16	
00071	2N3906	51	5	
00073	2N3055	1	1	
00106	2N4919	3	1	
00107	2N4923	2	1	
00108	2N5841	1	1	
00109	A210	3	1	
00112	MPS2369	12	3	
00115	2N4502	1	1	
00129	2N4403	12	3	
00130	2N5086	4	1	
00134	2N5089	1	1	
11724	E-H Selected	3	1	
11725	E-H Selected	2	1	
11757	E-H Selected	19	3	
11780	E-H Selected	2	1	
11781	E-H Selected	2	1	
Integrated Circuits				
665-00053	MC3000P	23	4	
00057	MC4006P	2	1	
00074	LM309K N.S.	1	1	
00078	MC3004P	4	1	
00079	N5741	7	2	
00080	74145	1	1	
00099	MC3021	28	4	

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Table 4-1 Recommended Spare Parts List (3 of 3)

SECTION 5

PARTS LIST

5-1 ORDERING INFORMATION

Replacement parts may be ordered through an E-H Representative or directly from the factory. To be certain of receiving the proper parts, always include the following information with the order:

- a. Model number and serial number of the instrument on which the parts will be installed.
- b. Schematic reference number and subassembly name, if applicable, for which the part is intended. If the part does not have a schematic reference, the description from the parts list should be used.
- c. E-H part number.

The warranty is given on page ii of this manual, opposite the Table of Contents. For factory repair, contact the Customer Service Department of E-H Research Laboratories, Inc., at the address given on the title page of this manual. Include the following information:

- a. Model number and serial number of the instrument on which the work is to be performed.
- b. Details concerning the nature of the malfunction; or, type of repair desired.

5-2 HOW TO USE THIS PARTS LIST

The pages of this parts list correspond to the physical subsections of the instrument (printed circuit boards, chassis

and subassemblies, miscellaneous hardware). Component locations can be determined from the assembly drawings and schematic diagrams in Section 6. Each component appears only once in the parts list. At the head of each page is listed the part number for the complete assembly or subassembly whose parts are listed. Care should be taken to locate malfunctions to the lowest possible level of replacement part and thus avoid the time and cost involved in “over-repair”.

5-3. MAJOR ASSEMBLIES

ASSEMBLY OR PART NO.	DESCRIPTION
251-21286	Front Panel Assembly
253-21287	Rear Panel Assembly
255-21288	Chassis Assembly
257-21289	Side Panel Assembly
261-21685	Frame Assembly, 5 1/4" x 18"
401-19756	Power Supply Regulator Assy
401-19977	Type B Clock Board Assy
401-22373	Delay & Width Bd Assy
401-20458	Type C Output Board Assy
401-21212	Parallel D/A Converter Assy
820-21290	Standard Accessories
350-21710	Completion Kit, Bench 5 1/4" x 18" or
350-21764	Completion Kit, Rack Mount 5 1/4" x 18" with Slides or
350-21711	Completion Kit, Rack Mount

ASSEMBLY NO. 251-21286DESCRIPTION FRONT PANEL ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
250-21061	Panel, Front	
630-00022	Switch	
	-HARDWARE-	
203-00037	#6-32x3/8 Lg OvalHMS 82°(6)	Prod Ref

ASSEMBLY NO. 253-21287DESCRIPTION REAR PANEL ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
252-22731	Panel, Rear	
144-22732	Silkscreen	Prod Ref
249-21283	Panel, Sub Assembly	
248-22734	Panel, Sub, BNC Conn. Transition	
396-00001	Fuse Holder	F101
398-00025	Fuse 2½ Amp S.B.	F101
570-00008	Fan	B101
570-00009	Grill	
700-00061	Receptacle, AC	J101
721-00013	Connector, BNC	J102-J107
	-HARDWARE-	
202-00311	Screw, 4-40x5/16 lg BHMS(10) Phil Dr.	Prod Ref
203-00313	Screw 6-32x5/16 BHMS (10)	Prod Ref
204-00008	Screw, 8-32x5/8 Lg BHMS(4)	Prod Ref
240-00001	#4-40 Kep Nut (2)	Prod Ref
240-00003	#8-32 Kep Nut (4)	Prod Ref
240-00002	#6-32 Kep Nut (4)	Prod Ref

ASSEMBLY NO. 249-21283DESCRIPTION PANEL, SUB, ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
248-21194	Panel, Sub	
706-21374	Cable Assy, 50 Pin	
706-21284	Cable Assy, 50 Pin	
706-21285	Cable Assy, 20 Pin	
144-21195	Silkscreen, Sub Panel	Prod Ref
460-00003	Ground Lug #4 (1)	Prod Ref
201-00004	Screw #3-48x $\frac{1}{2}$ BHMS (6)	Prod Ref
215-00002	Lockwasher #3 (6)	Prod Ref
240-00019	Nut #3-48 (6)	Prod Ref
758-00301	Wire, Bare Buss	Prod Ref
793-00315	Sleeving, TFE	Prod Ref

ASSEMBLY NO. 706-21374DESCRIPTION CABLE ASSEMBLY, 50 PIN

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
706-21374	Assembly Drawing	Prod Ref
700-00026	Connector, 50 Pin Amphenol	
400-22197	Paddle Board	
700-00125	3M #3426-0001 Transition, 50 Pin	
700-00122	3M 3416 Transition, 16 Pin Plug	
	Ribbon Cable, 50 Cond.	

ASSEMBLY NO. 706-21284DESCRIPTION CABLE ASSEMBLY, 50 PIN

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
700-00026	Connector, 50 Pin Amphenol	
400-22197	Paddle Bd	
700-00125	3M #3426-0001 50 Pin Transition	
700-00122	16 Pin Plug, 3M 3416	
	Ribbon	

ASSEMBLY NO. 706-21285DESCRIPTION CABLE ASSEMBLY, 20 PIN

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
700-00022	Connector, 24 Pin Amphenol	
400-22323	Paddle Bd	
700-00122	16 Pin Plug, 3M 3416	
700-00124	3M #3422-0001 Transition, 20 Pin	
	Ribbon Cable	

ASSEMBLY NO. 255-21288

DESCRIPTION CHASSIS ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
254-21063	Chassis	
144-21064	Silkscreen, Top	Prod Ref
144-21065	Silkscreen, Bottom	Prod Ref
258-13061	Cover, Terminal Strip	
262-21058	Bracket, Card Guides	
316-00073	Cap, El, 5500 μ f/40V	C301-304
316-00088	Cap, El, 17,000 μ f/40V	C305
376-00066	Diode, Westinghouse 368B	CR301,302
484-00023	Terminal Strip, Jumper	
484-00030	Card Guide	
484-00036	Terminal Strip	TB301
484-00037	Terminal Mtg. Strip	
484-00039	Card Guides	
484-00051	Feedthru Terminal ^{USECO} 4487B	
490-00001	Transistor Mtg. Kit	
596-00033	Resistor, 3.3 Ω $\frac{1}{2}$ W 5%	R308
597-00102	Resistor 1K 1W 5%	R302,304
597-00152	Resistor 1.5K 1W 5%	R301,303
598-00151	Resistor 150 Ω 2W 5%	R305

ASSEMBLY NO. 255-21288DESCRIPTION CHASSIS ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
610-00303	OHMITE #3723 Resistor 0.51 Ω 12W	R307
610-00135	OMI Resistor .1 Ω 5W w.w. T-5	R306
650-19604	Transformer, Power	T301
663-00115	Transistor, 2N4502	Q305
665-00074	IC LM309K N.S.	IC 301
663-00073	Transistor 2N3055	Q301-304
700-00126	34 Pin Header, Transition	J304
702-21074	Cable Harness Assy, Chassis	
318-00308	Cap, Tant 4.7 μ f 35V	C306
702-21075	Buss Wire List	Prod Ref
702-23010	Coax Wire List	Prod Ref
704-23139	Coax Cable Assy, Signal	
	Input (output Bd) Red	
704-23140	Coax Cable Assy, Signal	
	Input (Output Bd) Org.	
708-21076	Delay Line, 27ns	DL301
396-00201	Fuse Holder	XF301
398-00034	Fuse, 8 Amp Inst	F301
702-21389	Wire List, Xfmr & Component	Prod Ref
702-21390	Wire List, AC Pwr & Xfmr	Prod Ref

ASSEMBLY NO. 255-21288DESCRIPTION CHASSIS ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
	-HARDWARE-	
202-00311	Screw, 4-40x5/16 Lg BHMS (9)	Prod Ref
202-00305	Screw 4-40x $\frac{1}{2}$ Lg BHMS (38)	Prod Ref
203-00002	Screw 3-32x3/16 Lg BHMS (2)	Prod Ref
203-00304	Screw, 6-32x $\frac{1}{2}$ Lg FLTHMS (4)	Prod Ref
203-00313	Screw 6-32x5/16 Lg BHMS (16)	Prod Ref'
203-00315	Screw 6-32x5/16 lg FLTHMS (8)	Prod Ref
204-00004	Screw 8-32x3/8 Lg BHMS (6)	Prod Ref
215-00303	#8 Washer, Flat (2)	Prod Ref
240-00001	#4-40 Kepnut (38)	Prod Ref
240-00002	#6-32 Kepnut (18)	Prod Ref
240-00003	#8-32 Kepnut (6)	Prod Ref
420-00008	Grommet, 5/8 (2)	Prod Ref
420-00021	Grommet, 3/8 (1)	Prod Ref
420-00024	Grommet, 1/2 (1)	Prod Ref
475-00029	#6-32x $\frac{1}{4}$ lg Spacer Hex (2)	Prod Ref
405-00005	Cap. Clamp	XIC301-304
405-00034	Cap Clamp	XC 305

ASSEMBLY NO. 702-21074DESCRIPTION MAIN CHASSIS CABLE HARNESS ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
700-00022	Connector, 24 Pin Amphenol	J109
420-00006	Grommet 3/8 ID	
460-00006	Solder Lug #4 (1)	Prod Ref
460-00016	Solder Lug #6 (1)	Prod Ref
702-21074	Assembly Drawing	Prod Ref
702-21073	Wire List	Prod Ref

ASSEMBLY NO. 704-23139DESCRIPTION COAX CABLE ASSY, INPUT TO OUTPUT BD.
(RED)

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
704-23139	Assembly Drawing	Prod Ref
721-00308	Conn., Crimp-Right Angle	
776-16022	Wire RG174/U Red-Red	

ASSEMBLY NO. 704-23140DESCRIPTION COAX CABLE ASSY, INPUT TO OUTPUT BD.
(ORG)

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
704-23140	Assembly Drawing	Prod Ref
721-00308	Conn, Crimp-Right Angle	
776-16033	Wire, RG174/U Org-Org	

ASSEMBLY NO. 708-21076DESCRIPTION DELAY LINE ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
708-21076	Assembly Drawing	Prod Ref
240-00013	Clamp (2)	Prod Ref
786-00002	Wire, RG174 18'	
910-00076	Panduit Tie (10)	Prod Ref

ASSEMBLY NO. 257-21289DESCRIPTION SIDE PANEL ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
256-21067	Side Panel, Left	
256-21068	Side Panel, Right	
	-HARDWARE-	
203-00315	Screw #6-32x5/16 ^{FLTHMS} 100° (30)	Prod Ref
240-00002	Kepnut #6-32 (18)	Prod Ref

ASSEMBLY NO. 261-21685DESCRIPTION 5 1/4" X 18" FRAME ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
260-21501	Frame, Die Cast	
475-21505	Front Corner Post	
475-21514	Rear Corner Post	
425-21523	Handle	
146-21532	Filler, Handle	
276-21540	Overlay, Handle	
240-21606	Barnut	
274-21601	Spring, Cover Lift	
	HARDWARE-	
	Screw #2-56x3/8 Lg ^{FHTHMS 82°} (2)	Prod Ref
215-00023	#4 Washer Flat x9/32 OD (2)	Prod Ref
215-00001	Lock Washer Int. #2 (2)	Prod Ref
205-00044	Screw #10-24x3/4 LG ^{Taptite} (16)	Prod Ref

ASSEMBLY NO. 401-19756

DESCRIPTION POWER SUPPLY BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-19755	PC Board	
401-19756	Assembly Drawing	Prod Ref
140-19757	Schematic	Prod Ref
311-00021	Cap, Cerm .05 μ fd 75V	C1, C3, C5, C7
316-00044	Cap, El, 10 μ fd/25V	C2, C4, C6, C8
376-00062	Diode, Motorola 1N4720	CR4-11
374-12529	Diode, 12529	CR1
376-00034	Diode, 1N4005	CR3, CR12-19
595-00100	Resistor 10 Ω $\frac{1}{4}$ W 5%	
595-00101	Resistor 100 Ω $\frac{1}{4}$ W 5%	R1
595-00393	Resistor 39K $\frac{1}{4}$ W 5%	R18, R22
595-00102	Resistor 1K $\frac{1}{4}$ W 5%	R2
595-00068	Resistor 6.8 Ω $\frac{1}{4}$ W 5%	R4, R10, R16, R20
610-00088	Resistor .39 Ω 2W 5% w.w.	R3, R8, R9, R14 R15, R17, R19, R21
663-00070	Transistor, 2N3904	Q1-4
663-00131	Diode, SCR, 2N4441	CR2
665-00075	Regulator, IC, MFC 6030	
616-00715	Resistor 5.11K $\frac{1}{4}$ W 5% MF	R7, R13
616-00713	Resistor 1.82K $\frac{1}{4}$ W 1% MF	R5, R11

ASSEMBLY NO. 401-19977DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-19976	PC Board	
401-19977	Assembly Drawing	Prod Ref
140-19978	Schematic	Prod Ref
311-00009	Cap, Cerm 500pf 1KV 10%	C31
311-00007	Cap, Cerm 100pf 1KV 10%	C13
311-00003	Cap, Cerm 25pf	C3
311-00010	Cap, Cerm .001 μ f 1KV 10%	C9,24, 32-34
311-00034	Cap, Cerm .1 μ f 50V	C2
311-00067	Cap, .001 μ f Hi-Q	C16
311-00074	Cap, Cerm .01 μ f 100V	C1,5,7, 10-12,15, 19-21,23, 27, 28
311-00333	Cap, Dipped Mica 62pf	C4
312-14972	Cap, Chip 0.1	C6
318-00005	Cap, Tant 10 μ f 20V	C8,14,17, 18,22,29
335-00001	Choke 1.5 μ h	L4-7
335-23309	Choke Assy, 5T	L1,2
335-00019	Choke, .47 μ h	L3
374-11761	Diode, MP	CR20A&B, CR29A&B, CR33A&B
374-11732	Diode, MP 1N751A	
376-00022	Diode, 1N914B	CR1-4,6-17 25-28

ASSEMBLY NO. 401-19977DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
376-00031	Diode, 1N270	CR 32
376-00700	Diode, MBD101	CR5,18,19, 21-24
551-00068	Potentiometer 100 Ω	R68
551-00069	Potentiometer 100K	R26
551-00071	Potentiometer 500 Ω	R53
594-00100	Resistor 10 Ω 1/8W 5%	R3, 7,9, 62, 45
		58,63,66, 72,81,82
594-00104	Resistor 100K 1/8W 5%	R8
594-00150	Resistor 15 Ω 1/8W 5%	R42
594-00300	Resistor 30 Ω 1/8W 5%	R6,10,14, 17
595-00100	Resistor 10 Ω 1/2W 5%	R91,108, 112,113,129
		130,131
595-00101	Resistor 100 Ω 1/2W 5%	R27,84, 94,103
595-00103	Resistor 10K 1/2W 5%	R96,132 126,128
595-00121	Resistor 120 Ω 1/2W 5%	R44
595-00122	Resistor 1.2K 1/2W 5%	R61,70,
595-00123	Resistor 12K 1/2W 5%	R22

ASSEMBLY NO. 401-19977DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R13,15,30, 33,50,76, 78,86,90, 95,97,102
595-00151	Resistor 150 Ω $\frac{1}{2}$ W 5%	R12
595-00152	Resistor 1.5K $\frac{1}{2}$ W 5%	R38,41,64, 67,75,80
595-00153	Resistor 15K $\frac{1}{2}$ W 5%	R20
595-00182	Resistor 1.8K $\frac{1}{2}$ W 5%	R99,106
595-00201	Resistor 200 Ω $\frac{1}{2}$ W 5%	R35,119,123 125,127
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R77
595-00240	Resistor 24 Ω $\frac{1}{2}$ W 5%	R120-122
595-00242	Resistor 2.4K $\frac{1}{2}$ W 5%	R87-89
595-00271	Resistor 270 Ω $\frac{1}{2}$ W 5%	R46,57
595-00272	Resistor 2.7K $\frac{1}{2}$ W 5%	R56
595-00302	Resistor 3K $\frac{1}{2}$ W 5%	R31,32,34 R115 73,74,114
595-00332	Resistor 3.3K $\frac{1}{2}$ W 5%	R28,105
595-00391	Resistor 390 Ω $\frac{1}{2}$ W 5%	R43,98
595-00392	Resistor 3.9K $\frac{1}{2}$ W 5%	R85,101
595-00471	Resistor 470 Ω $\frac{1}{2}$ W 5%	R29,36,37, 39,116
595-00472	Resistor 4.7K $\frac{1}{2}$ W 5%	R100,107
596-00432	Resistor 4.3K $\frac{1}{2}$ W 5%	R16
595-00750	Resistor 75 Ω $\frac{1}{2}$ W 5%	R117

ASSEMBLY NO. 401-19977DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00820	Resistor 82Ω ½W 5%	R79,83
595-00821	Resistor 820Ω ½W 5%	R111
595-00910	Resistor 91Ω ½W 5%	R65,71,92, 93,109,110
595-00912	Resistor 9.1K ½W 5%	R104
597-00391	Resistor 390Ω 1W 5%	R59
597-00511	Resistor 510Ω 1W 5%	R54
616-00308	Resistor 402Ω 1/8W 1% MF	R2,4,49,51
616-00317	Resistor 1.5K 1/8W 1% MF	R55
616-00349	Resistor 100K 1/8W 1% MF	R25
616-00705	Resistor 221Ω 1/8W 1% MF	R60
616-00714	Resistor 3.32K 1/8W 1% MF	R24
616-00715	Resistor 5.11K 1/8W 1% MF	R23
616-00723	Resistor 2.37K 1/8W 1% MF	R47
616-00724	Resistor 3.57K 1/8W 1% MF	R48,52,69
617-00003	Resistor 2K ½W 1% MF	R18
617-00007	Resistor 2.21K ½W 1% MF	R1,5,11
617-00065	Resistor 18.2K ½W 1% MF	R21
617-00004	Resistor 249Ω ½W 1% MF	R118
616-00027	Resistor 2.74K 1/8W 1% MF	R19

ASSEMBLY NO. 401-19977DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
663-00070	Transistor 2N3904	Q11,12,17, 20,26-28
		37-40
663-00071	Transistor 2N3906	Q1,13,16, 25,43,44,
		52
663-00112	Transistor MPS2369	Q7,14,15, 18,19,21-24
		29,30,33-36 ,49,50,51
663-11757	Transistor	Q2-6,8-10 31,32,41,
		42,45-48
665-00037	IC MC849P	IC13,14
665-00053	IC MC3000P	IC9-11
665-00057	IC MC4006P	IC 8
665-00062	IC MC 3006P	IC 12
665-00076	IC MC7490P or SN7490N	IC 1-6
665-00077	IC SN74196N	IC 7

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22372	PC Board	
401-22373	Assembly Drawing	Prod Ref
140-22374	Schematic	Prod Ref
311-00003	Cap., Cerm., 25pf	C44
311-00016	Cap, Cerm .001 μ f 1KV GMV	C1,2,9,11, 14,18,19, 21,33-36, 38,39
311-00020	Cap, Mono .47 μ f/25V	C10,15
311-00028	Cap, Cerm 200pf	C40,43
311-00034	Cap, Mono .1 μ f/50V	C3,7,12, 23,37
311-00064	Foil Tab Cap, Cerm 100pf 500V 10T	C4,13
311-00069	Foil Tab Cap, Cerm .005 μ f 500V 10%	C5,6,16,17
311-00073	Foil Tab Cap, Cerm 500pf 500V 10%	C24
311-00084	Cap, Mica 130pf 1%	C8,22
318-00005	Cap, Tant 10 μ f 20V	C30-32
320-00069	Cap, Mylar .018 μ f 200V 1%	C25,29
320-00070	Cap, Mylar 1.8 μ f 200V 1%	C26,28
320-00077	SEI #22 μ -A162G Cap, Mylar .0016 μ f 50V 2%	C20,27
318-00042	$\pm 10\%$ Cap, 180 μ f 6WVDC Sprague	C41,42
335-00001	Choke 1.5 μ h	L1-3
374-00080	Diode, 1N747A	CR15

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
374-12529	Diode, Zener	CR27
374-11797	Diode, MP 1N746A	CR4A&B
376-00022	Diode, 1N914B	CR1,18-20 30,43-45, 50,51
376-00031	Diode, 1N270	CR46-49
376-11764	Diode	CR2,3,7,12 21,22,24, 32,37,40
376-00700	Diode, MBD101	CR8-11,13, 14,16,17, 23,25,26, 28,29,31, 33-36,38, 39,41,42,6
551-00062	Helitrim 62P Potentiometer 10K	R136,179
551-00070	Helitrim 72XW Potentiometer 200 Ω	R17,60
551-00071	Helitrim 72XW Potentiometer 500 Ω	R21,26,46 52
551-00051	Potentiometer 5K Helitrim	R138,185
595-00036	Resistor 3.6 Ω $\frac{1}{4}$ W 5%	R80,97
595-00051	Resistor 5.1 Ω $\frac{1}{4}$ W 5%	R83,84, 95,96,126, 127,174, 176,219,218
595-00100	Resistor 10 Ω $\frac{1}{4}$ W 5%	R1,25,51
595-00180	Resistor 18 Ω 1/4W 5%	R128,177

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R31,56,111, 113,116-119
		121,122,124, 133,156,167
		168,175,183, 192-195,
		200,202, 208-210,213
		216
595-00101	Resistor 100 Ω $\frac{1}{2}$ W 5%	R4,6,13,33 35,42,53,69
		72,93, 104,108,217
595-00103	Resistor 10K $\frac{1}{4}$ W 5%	R115 120,131,142
		144,164-166 170,172,173
		190,191,196 197,204-206
		212,140, 225-229
595-00104	Resistor 100K $\frac{1}{2}$ W 5%	R82,169
595-00105	Resistor 1M $\frac{1}{2}$ W 5%	R125,129, 171,180
		221-224
595-00153	Resistor 15K $\frac{1}{2}$ W 5%	R10,38,49, 132,161,188
		189,203,211 114
595-00162	Resistor 1.6K $\frac{1}{2}$ W 5%	R7,37, 214,220
595-00182	Resistor 1.8K $\frac{1}{2}$ W 5%	R5,
595-00200	Resistor 20 Ω $\frac{1}{2}$ W 5%	R30,98
595-00201	Resistor 200 Ω $\frac{1}{2}$ W 5%	R73,91

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00202	Resistor 2K $\frac{1}{2}$ W 5%	R158, 159
595-00203	Resistor 20K $\frac{1}{2}$ W 5%	R162
595-00221	Resistor 220 Ω $\frac{1}{2}$ W 5%	R78, 148, 149
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R23, 48, 145, R198 199, 146, 163
595-00241	Resistor 240 Ω $\frac{1}{2}$ W 5%	R11, 41
595-00301	Resistor 300 Ω $\frac{1}{2}$ W 5%	R66
595-00302	Resistor 3K $\frac{1}{2}$ W 5%	R85, 100
595-00391	Resistor 390 Ω $\frac{1}{2}$ W 5%	R101, 103, 109 157, 160
595-00392	Resistor 3.9K $\frac{1}{2}$ W 5%	R207, 215
595-00431	Resistor 430 Ω $\frac{1}{2}$ W 5%	R67
595-00471	Resistor 470 Ω $\frac{1}{2}$ W 5%	R106
595-00510	Resistor 51 Ω $\frac{1}{2}$ W 5%	R15, 29, 44, 50
595-00681	Resistor 680 Ω $\frac{1}{2}$ W 5%	R92
595-00682	Resistor 6.8K $\frac{1}{2}$ W 5%	R32, 57
595-00750	Resistor 75 Ω $\frac{1}{2}$ W 5%	R86, 87
595-00752	Resistor 7.5K $\frac{1}{2}$ W 5%	R8, 36, 110
595-00820	Resistor 82 Ω $\frac{1}{2}$ W 5%	R74, 75, 141, 153
595-00910	Resistor 91 Ω $\frac{1}{2}$ W 5%	R19, 58, 70
595-00911	Resistor 910 Ω $\frac{1}{2}$ W 5%	R9, 39
595-00912	Resistor 9.1K $\frac{1}{2}$ W 5%	R81, 99

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
596-00102	Resistor 1K $\frac{1}{2}W$ 5%	R112, 123, 130 181, 182, 187
596-00122	Resistor 1.2K $\frac{1}{2}W$ 5%	R12, 40
596-00391	Resistor 390 Ω $\frac{1}{2}W$ 5%	R63
596-00361	Resistor 360 Ω $\frac{1}{2}W$ 5%	R89
596-00510	Resistor 51 Ω $\frac{1}{2}W$ 5%	R107
596-00511	Resistor 510 Ω $\frac{1}{2}W$ 5%	R152, 154
596-00561	Resistor 560 Ω $\frac{1}{2}W$ 5%	R105
596-00821	Resistor 820 Ω $\frac{1}{2}W$ 5%	R68, 71, 76, 77 90, 143, 147, 150, 151, 155
596-00751	Resistor 750 Ω $\frac{1}{2}W$ 5%	R79, 88, 94, 102
595-00183	Resistor 18K $\frac{1}{4}W$ 5%	R65
616-00034	Resistor 1K 1/8W 1% MF	R2, 134, 135, 186, 201
616-00035	Resistor 2K 1/8W 1% MF	R3
616-00037	Resistor 10K 1/8W 1% MF	R24, 34
616-00307	Resistor 348 Ω 1/8W 1% MF	R18, 61
616-00707	Resistor 392 Ω 1/8W 1% MF	R28, 55
616-00714	Resistor 3.32K 1/8W 1% MF	R27, 54
616-00720	Resistor 511 Ω 1/8W 1% MF	R14, 43
616-00724	Resistor 3.57K 1/8W 1% MF	R22, 47
616-00712	Resistor 1.1K 1/8W 1% MF	R139, 184

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
617-00044	Resistor 845Ω $\frac{1}{2}$ W 1% MF	R20,45
663-00070	Transistor 2N3904	Q1,5,9,10, 14,17,18,28 44,48,49,53 54,55,60,61 64,65,67, 71,74
663-00071	Transistor 2N3906	Q2-4,6-8,11 13,15,16,45 50-52,63, 57-59,62, 68,70,73
663-00112	Transistor MPS2369	Q12,19,25, 27,29,30, 33,34,38, 39
663-00129	Transistor 2N4403	Q42,43,46, 47,56,66, 69,72
665-00078	IC MC 3004P	IC1,3,4,6
665-00057	IC MC 4006P	IC 2,5
704-23336	Clipping Line Assy	CL 1-4
663-11757	Transistor	Q20-24,26 31,32,35-37 40,41
616-00336	Resistor 15K, 1% MF	I38 R16,59,137

ASSEMBLY NO. 401-22373DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
311-00035	Cap, Cerm 15pf	C45
595-00432	Resistor 4.3K $\frac{1}{2}$ W 5%	R62,64
	-HARDWARE-	
	Clamp, Cable (1)	Prod Ref
	Screw, 2-56 (1)	Prod Ref
	Nut, 2-56 (1)	Prod Ref

ASSEMBLY NO. 704-23336DESCRIPTION CLIPPING LINE, TIMING BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
704-23336	Assembly Drawing	Prod Ref
776-00012	RG 195/U Coax X 10"(93Ω)	
721-23036	Connector, Termination	
272-23037	Sleeve, Crimp	
795-00039	Shrink Tubing	

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-20457	PC Board	
401-20458	Assembly Drawing	Prod Ref
140-20459	Schematic	Prod Ref
311-00002	Cap, Cerm 20pf 1KV	C41, 42
311-00005	Cap, Cerm 30pf 1KV 10%	C1, 10
311-00006	Cap, Cerm, 50pf 10%	C54
311-00007	Cap, Cerm 100pf 10%	C52, 53
311-00010	Cap, Cerm .001μf	C2, 4, 5, 37, 45
311-00011	Cap, Cerm .005μf	C3
311-00034	Cap, Cerm .1μf 50V	C16, 26, 32, 33, 46, 44
311-00068	Cap, Cerm 33pf Hi-Q	C19
311-00074	Cap, Cerm .01μf 100V	C17, 18, 36, 47-50
311-00097	Cap, Mica 56pf 5%	C11
311-00098	Cap, Mica, 620pf 1%	C9
312-14971	Cap, Chip 390pf	C13
312-14972	Cap, Chip .1μf	C12, 15, 24, 25, 38
312-14974	Cap, Chip .01	C14
311-00008	Cap., Cerm 150pf 10%	C39, 51

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
318-00005	Cap, Tant 10 μ f 20V	C27-31, 35
318-00019	Cap, Tant, 47 μ f 20V	C20-23
318-00038	Cap, Tant 5.6 μ f 35V	C34, 40
320-00074	Cap, Poly .075pf 1%	C7
320-00076	Cap, Poly .75pf 1%	C6
326-00026	Cap, Poly 6750pf 1%	C8
332-00010	Cap, Variable 2.5-9pf	C43
335-00022	Choke 1 μ h	L17-21
335-10956	Choke Assembly	L1, 3
335-19184	Choke 20T (2) 3D3	L13, 14
335-14686	Choke 5T (1) 4C4	L4, 2, 10, 12
335-17303	Choke 10T (1) 3E2A	L11
335-23467	Choke 10T (4) 4C4	L15
335-24784	Choke Assembly	L16
361-00012	Core, 4C4	L5
374-00022	Diode, Zener 1N751A	CR22
374-00037	Diode, Zener 1N759A	CR9

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
374-00044	Diode, 1N749A	CR11
374-11733	Diode, MP 1N759A	CR12 A&B
374-11761	Diode MP	CR7 A&B
376-00022	Diode 1N914B	CR1-4, 6, 10, 14-21, 23-26, 32-41, 43
376-22925	Diode Sel. MBD 101	CR29-31
490-00020	Heat Sink	XQ27
490-00041	Pad, Transistor Insulator T0-18	XR129
490-00045	Heat Sink (IERC-PA1-1CB)	XQ42, 43, 83
490-00046	Heat Sink (IERC-PB1-3CB)	XQ26
490-00048	Heat Sink (Wake. 26010SH5)	XQ28, 59, 60
490-16574	Heat Sink Plate	XQ26
490-17026	Heat Sink	XQ37, 62
490-17108	Heat Sink Plate	XQ37, 62
490-23128	Heat Sink Plate	XR129, XQ42, 43, 83
376-00700	Diode MBD101	CR 42
495-00027	Amp Pins	XQ27, 28, 57-60
496-00029	Pad, Transistor Insulator T0-5	

ASSEMBLY NO. 401-20458

DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
551-00038	Pot, 2K	R201, 204
551-00070	Pot, 200 Ω	R104
551-00071	Pot. 500 Ω	R94
551-00072	Pot. 50 Ω	R71
551-00073	Pot. 1K	R31, 55
551-00074	Pot. 2K	R7
551-00075	Pot. 50K	R25, 34, 65
551-00076	Pot. 500K	R57, 216
584-00018	Relay, Zestron 226-12-1A	K5
584-00019	Relay, Hi-G	K1-4
594-00039	Resistor 3.9 Ω 1/8W 5%	R164
594-00051	Resistor 5.1 Ω 1/8W 5%	R128
594-00056	Resistor 5.6 Ω 1/8W 5%	R75
594-00103	Resistor 10K 1/8W 5%	R218
594-00560	Resistor 56 Ω 1/8W 5%	R95, 110, 111
594-00750	Resistor 75 Ω 1/8W 5%	R117, 118
595-00027	Resistor 2.7 Ω 1/4W 5%	R8
595-00036	Resistor 3.6 Ω 1/4W 5%	R44, 47

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00100	Resistor 10 Ω 1/4W 5%	R40, 60, 72, 120, 125, 198, 199, 214
595-00102	Resistor 1K 1/4W 5%	R41, 59, 79, 80, 86, 102, 154, 155, 169, 206
595-00103	Resistor 10K 1/4W 5%	R21, 37, 156- 158, 166-168
595-00105	Resistor 1M 1/4W 5%	R162, 163, 211
595-00104	Resistor 100K 1/4W 5%	R33
595-00124	Resistor 120K 1/4W 5%	R56
595-00152	Resistor 1.5K 1/4W 5%	R183, 186, 188, 190
595-00200	Resistor 20 Ω 1/4W 5%	R61, 62
595-00201	Resistor 200 Ω 1/4W 5%	R9
595-00202	Resistor 2K 1/4W 5%	R78, 91
595-00182	Resistor 1.8K 1/4W 5%	R222
595-00203	Resistor 20K 1/4W 5%	R10, 219
595-00222	Resistor 2.2K 1/4W 5%	R14, 19, 88, 107, 150
595-00271	Resistor 270 Ω 1/4W 5%	R58, 165
595-00300	Resistor 30 Ω 1/4W 5%	R66, 127
595-00302	Resistor 3K 1/4W 5%	R101
595-00330	Resistor 33 Ω 1/4W 5%	R42, 43
595-00332	Resistor 3.3K 1/4W 5%	R5, 92, 106

ASSEMBLY NO. 401-20458

DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00333	Resistor 33K 1/4W 5%	R11, 12, 49
595-00361	Resistor 360 Ω 1/4W 5%	R73, 74
595-00362	Resistor 3.6K 1/4W 5%	R76
595-00390	Resistor 39 Ω 1/4W 5%	R63
595-00391	Resistor 390 Ω 1/4W 5%	R174, 178, 208
595-00393	Resistor 39K 1/4W 5%	R196
595-00223	Resistor 22K 1/4W 5%	R223-225
595-00471	Resistor 470 Ω 1/4W 5%	R191-194, 207
595-00472	Resistor 4.7K 1/4W 5%	R195, 197
595-00510	Resistor 51 Ω 1/4W 5%	R15, 17, 18, 99, 215
595-00511	Resistor 510 Ω 1/4W 5%	R100
595-00560	Resistor 56 Ω 1/4W 5%	R112
595-00563	Resistor 56K 1/4W 5%	R23, 27, 35, 50, 67
595-00680	Resistor 68 Ω 1/4W 5%	R77
595-00682	Resistor 6.8K 1/4W 5%	R83, 87, 103
595-00683	Resistor 68K 1/4W 5%	R147-149, 151-153
595-00822	Resistor 8.2K 1/4W 5%	R69
595-00910	Resistor 91 Ω 1/4W 5%	R64
595-00911	Resistor 910 Ω 1/2W 5%	R213, 217

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
596-00102	Resistor 1K 1/2W 5%	R108
596-00121	Resistor 120 Ω 1/2W 5%	R113
596-00122	Resistor 1.2K 1/2W 5%	R16, 180, 209
596-00241	Resistor 240 Ω 1/2W 5%	R182, 184, 187, 189
596-00681	Resistor 680 Ω 1/2W 5%	R170-173
597-00241	Resistor 240 Ω 1W 5%	R45
597-00431	Resistor 430 Ω 1W 5%	R126
597-00621	Resistor 620 Ω 1W 5%	R181
598-00131	Resistor 130 Ω 2W 5%	R210
610-00019	Resistor 10 Ω 3W w.w.	R179
610-00136	Resistor 18 Ω 3W w.w.	R89, 109
616-00331	Resistor 7.5K 1% MF	R176
616-00332	Resistor 9.09K 1/8W 1% MF	R81, 200
616-00704	Resistor 162 Ω 1/4W 1% MF	R32
616-00714	Resistor 3.32K 1/4W 1% MF	R3
616-00726	Resistor 1.5K 1/4W 1% MF	R53

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
617-00002	Resistor 1K 1/4W 1% MF	R24,38,54, 84,85,93, 202,205
617-00003	Resistor 2K 1/4W 1% MF	R22,36
617-00010	Resistor 4.02K 1/4W 1% MF	R203
617-00011	Resistor 4.99K 1/4W 1% MF	R29
617-00012	Resistor 10K 1/4W 1% MF	R2,13,20, 26,39
617-00013	Resistor 20K 1/4W 1% MF	R28,48,51, 68
617-00035	Resistor 8.06K 1/4W 1% MF	R4,6
617-00036	Resistor 16.2K 1/4W 1% MF	R1
617-00023	Resistor 1.1K 1/4W 1% MF	R177
617-00047	Resistor 5.62K 1/4W 1% MF	R90
617-00056	Resistor 2.49K 1/4W 1% MF	R52
617-00064	Resistor 4.64K 1/4W 1% MF	R30
617-00065	Resistor 18.2K 1/4W 1% MF	R82
617-00057	Resistor 19.1K 1/4 W 1% MF	R212
617-00089	Resistor 130 Ω 1/4W 1% MF	R70
618-00116	Resistor 10 Ω 1/2W 1%MS150	R96-98, 114-116
619-00006	Resistor 25.5 Ω 1W MS220	R119,124
619-00007	Resistor 51 Ω 1W 1% MS210	R122,123
617-00322	Resistor 887 Ω 1/4W 1% MF	R105

ASSEMBLY NO. 401-20458

DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
622-00050	Resistor 75Ω 2W 1% MS220	R130, 134
622-00051	Resistor 150Ω 2W 1% MS220	R135, 136
622-00052	Resistor 93.1Ω 2W 1% MS220	R131-133
622-00053	Resistor 165Ω 2W 1% MS220	R137-142, 145, 146
622-00054	Resistor 82.5Ω 2W 1% MS220	R143, 144
623-00001	Resistor 65Ω 15W 1% MP312	R129
595-	Resistor, Factory Select	R121, 175
*651-12570	Transformer	T1
*651-19186	Transformer, Balun	T2
663-00070	Transistor 2N3904 NPN	Q3, 6, 10, 13, 14, 17, 22, 33, 35, 39, 40, 45, 48, 53, 61, 63-66, 73-75, 86
663-00071	Transistor 2N3906 PNP	Q1, 2, 4, 5, 11, 16, 20, 23, 25, 30-32, 34, 36, 44, 41, 46, 47, 52, 67-72, 82, 84, 88, 89
663-00106	Transistor 2N4919	Q21, 26, 43
663-00107	Transistor 2N4923	Q42, 83
663-00108	Transistor 2N5841	Q27
663-00109	Transistor A210	Q28, 59, 60
663-00112	Transistor MPS 2369	Q50, 51
663-00129	Transistor 2N4403	Q76-79

ASSEMBLY NO. 401-20458DESCRIPTION TYPE C OUTPUT BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
663 -00130	Transistor 2N5086	Q9, 15, 38, 49
663 -11724	Transistor	Q12, 29, 85
663 -11725	Transistor	Q54, 87
663 -11757	Transistor	Q7, 8, 18, 19, 55, 56
663 -11780	Transistor 2N5635	Q37, 62
663 -11781	Transistor 11749 Sel.	Q57, 58
663 -00134	Transistor 2N5089	Q35
665 -00053	IC MC 3000P	IC2, 3
665 -00080	IC 74145	IC 1
704 -23138	Output Cable Assembly	J108
715 -23086	Connector Strip Line	
721 -00052	Connector, Micon	J1, 2
410 -00020	Component Clip (1)	Prod Ref
484 -00051	Washer, Teflon (1)	Prod Ref

ASSEMBLY NO. 355-24784DESCRIPTION CHOKE ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
335 -24784	Assembly Drawing	Prod Ref
361 -00014	Core, Green 4C4	
	Wire #24 Polythermaleze	Prod Ref

ASSEMBLY NO. 401-21212DESCRIPTION PARALLEL D/A CONVERTER BOARD BCD
ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-21209	PC Board	
401-21212	Assembly Drawing	Prod Ref
140-21213	Schematic	Prod Ref
311-00001	Cap, Cerm 10pf 10V	C6
311-00074	Cap, Cerm .01μf/100V	C1,3,5
318-00005	Cap, Tant, 10μf 20V	C2,4
495-00059	IC Socket, 16 Pin	J1
496-00043	Transistor Pad	XIC1
551-00035	Potentiometer 500Ω Beckman 79PR	R43
551-00040	Potentiometer 1K, Beckman 79PR	R40
595-00100	Resistor 10Ω ½W 5%	R47,48
595-00102	Resistor 1K ½W 5%	R2
595-00165	Resistor 1.6M ½W 5%	R5
595-00222	Resistor 2.2K ½W 5%	R3,16-39
595-00335	Resistor 3.3M ½W 5%	R4
595-00394	Resistor 390K ½W 5%	R7
595-00512	Resistor 5.1K ½W 5%	R1
595-00682	Resistor 6.8K ½W 5%	R46

ASSEMBLY NO. 401-21212DESCRIPTION PARALLEL D/A CONVERTER BOARD BCD
ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00824	Resistor 820K $\frac{1}{2}$ W 5%	R6
611-00001	Resistor 4K .05% Vishay V53-1	R15
611-00002	Resistor 8K .1% Vishay V53-1	R14
611-00003	Resistor 16K .1% Vishay V53-1	R13
611-00004	Resistor 32K .1% Vishay V53-1	R12
616-00015	Resistor 165K 1/8W 1% MF	R9
616-00016	Resistor 316K 1/8W 1% MF	R8
616-00017	Resistor 3.32K 1/8W 1% MF	R45
616-00330	Resistor 6.19K 1/8W 1% MF	R41
616-00332	Resistor 9.09K 1/8W 1% MF	R42
617-00014	Resistor 40.2K $\frac{1}{2}$ W 1% MF	R11
617-00071	Resistor 80.6K $\frac{1}{2}$ W 1% MF	R10
616-00326	Resistor 4.42K 1/8W 1% MF	R44
663-00070	Transistor 2N3904	Q1-13
665-00053	IC MC 3000P	IC 6-8
665-00079	IC N5741	IC 1
665-00099	IC MC 3021	IC 2-5

ASSEMBLY NO. 820-21290DESCRIPTION STANDARD ACCESSORIES

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
148	Manual	
786-00002	Power Cord	
800-00032	Envelope	
700-00034	Amphenol, 50 Pin Connector	
700-00024	Connector, 24 Pin Amphenol	
401-23973	Extender Bd Assy 44 Pin	Optional
401-23975	Extender Bd Assy 88 Pin	Optional

ASSEMBLY NO. 350-21710DESCRIPTION BENCH COMPLETION KIT 5½" X 18"

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
258-21618	Cover, Top & Bottom	
258-21559	Side Cover, Left	
258-21560	Side Cover, Right	
417-00007	Foot, Black	
	-HARDWARE-	
203-00059	#6-32 Screw Blue Hd BHMS (4)	Prod Ref
203-00060	#6-32 FLTHMS Blue Hd Screw (4)	Prod Ref
203-00016	#6-32 Screw FILHMS X 5/8 Lg	Prod Ref

ASSEMBLY NO. 350-21764DESCRIPTION RACK COMPLETION KIT W/SLIDES
5½" X 18"

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
262-21548	Bracket, Rack Mtg Ear	
258-21555	Cover, Top & Bottom	
475-21600	Spacer, Slide Mtg	
*284-16917	Chassis Slide Kit, 20"Std	
	-HARDWARE-	
203-00010	#6-32x3/8 Screw FLTHMS 100°	Prod Ref
220-00041	#8-32 Nut-Sert	Prod Ref

ASSEMBLY NO. 350-21711

DESCRIPTION RACK COMPLETION KIT 5 1/4" x 18"

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
262-21548	Bracket, Rack Mtg. Ear	
258-21555	Cover, Top & Bottom	
475-21600	Spacer, Slide Mtg.	
	- Hardware -	
203-00010	#6-32 x 3/8 FLTHMS 100° ⁽¹²⁾ Screw	Prod Ref
204-0004	#8-32 x 3/8 BHMS Screw (12)	Prod Ref
220-00041	#8-32 Nut-Sert (12)	Prod Ref

SECTION 6

DRAWINGS

6-1 GENERAL INFORMATION

This section of the manual contains drawings of the subassemblies and circuits in the E-H Model 1501A Pulse Generator. The drawings contain the component circuit designators and show the location of the wiring terminals. The theory of operation is located in Section 3 and the parts list is located in Section 5.

6-2 SCHEMATIC DIAGRAMS

In the schematics the convention of signal-flow from left to right is followed wherever practicable. Component symbology and nomenclature follow generally-accepted practices. Resistance is given in ohms. Capacitor values less than 1 are in microfarads and more than 1 are in picofarads unless otherwise labeled.

b. Frequency Range Verification

This procedure checks the operating range of the internal clock.

(1) Set all front-panel PROGRAM MODE switches to the LOCAL position.

(2) Set front-panel switches as follows:

CLOCK	INT
GATE	OFF
PULSE MODE	SINGLE
WIDTH	10 ns
DELAY	10 ns
RAMPS	999 x3 V/ns
AMPLITUDE	
POLARITY	N+
RANGE	5.0V
%of RANGE	50.00
OFFSET	OFF

(3) Connect Model 1501A trigger output to input of Universal Counter-Timer. Set Counter-Timer for frequency measurement.

(4) Measure the Model 1501A output frequency at several points on each range. The frequency should be within +5% of the setting. At low frequencies, the period mode of the Counter-Timer should be used for best resolution.

c. Width and Delay Verification.

This procedure checks the operation and calibration accuracy of the pulse width and pulse delay circuits.

(1) If a sampling oscilloscope with internal triggering is available, connect the trigger output of the Model 1501A to one channel of the oscilloscope and the main pulse output to the other channel. Connect the two coaxial attenuators in series with the sampling oscilloscope input to prevent damage to the oscilloscope. If the AMC Model 1100 is used, connect the pulse output to the oscilloscope input and the trigger output to the oscilloscope trigger input.

(2) Procedure using internally triggered oscilloscope. Trigger oscilloscope on pulse generator trigger output trace. Measure the delay between the leading edge of the trigger waveform and the leading

edge of the main pulse. The delay measured should be within $\pm 5\%$ of the setting, except on the 10 ms - 100 ms and 100 ms - 1 s ranges, where the accuracy is $\pm 15\%$. It may be necessary to use the time interval mode of the counter-timer to measure long delays. When using a sampling oscilloscope, the measurement error due to the oscilloscope must be taken into account when measuring time.

(3) Procedure using AMC 1100. Set PULSE MODE to DOUBLE. Adjust delay control Model 1100 to display trailing edge of first pulse and the entire second pulse. The pulse width may have to be adjusted to display the trailing edge of the first pulse. Set the Model 1100 to measure the time interval between the 50% points of the trailing edge of the two pulses. Measure the time interval at points on each range by setting the DELAY control. The interval measured should be within $\pm 5\%$ of the setting, except on the 10 ms - 100 ms and 100 ms - 1 s ranges, where the accuracy is $\pm 15\%$. It will be necessary to use the counter-timer as indicated above on the longer delay ranges.

NOTE

It will be necessary to change the pulse frequency as the delay setting is increased. use a frequency that will give approximately 50% duty cycle.

(4) Trigger sampling oscilloscope externally from Model 1501A trigger output. Set delay control and oscilloscope sweep time to display the entire pulse. Measure the pulse width between the 50% points on the leading and trailing edges. It should be within $\pm 5\%$ of the setting, except on the 10 ms - 100 ms and 100 ms - 1 s ranges, where the accuracy is $\pm 15\%$. It will be necessary to use the counter-timer to measure the width. Keep delay and width within approximately 50% of the period, as noted above.

d. Amplitude and Offset Verification

This procedure checks the operation of the amplitude and offset circuits.

(1) Set Model 1501A controls as follows:

FREQUENCY	50 kHz
DELAY	as required
WIDTH	50 ns
RAMPS	999 x 3 V/ns

PULSE MODE SINGLE
OFFSET OFF,0000V
AMPLITUDE
 RANGE 10.0V
 % OF RANGE 99.95

All other controls should be left in the positions specified in step b(2) above.

(2) Connect the Model 1501A pulse output (through the two coaxial attenuators in series) to the sampling oscilloscope input. Connect the trigger output to the trigger input of the oscilloscope. Trigger the oscilloscope and adjust the DELAY control so that the pulse waveform appears on the screen.

(3) Measure the peak-to-peak pulse amplitude (excluding any overshoot or ringing). It should be 10 V $\pm 5\%$ (9.05 V + 10.05 V).

(4) Check the programmed amplitude at other points on the 10.0 V range. It should be within the tolerance specified.

(5) Set the RANGE switch to the other positions. The amplitude should decreased by a factor of two on each range.

(6) Set the GATE switch to the ON position. This disables the pulse output. Connect the output of the Model 1501A to the input of the digital voltmeter, using a 50-ohm termination at the digital voltmeter input.

(7) Set the OFFSET switch to POS and measure the offset voltage at several points over the range. The voltage measured should be within $\pm 5\%$ of the setting.

(8) Set the OFFSET switch to the NEG and repeat step(7) above.

e. Rise and Fall Time Verification

This procedure checks the range and programming accuracy of the rise and fall ramps.

(1) Connect the output of the Model 1501A to the input of the sampling oscilloscope. Connect the two coaxial attenuators in series with the sampling oscilloscope input. Connect the trigger output to the oscilloscope trigger input.

- (2) Set Model 1501A controls as follows:

FREQUENCY	50 kHz
WIDTH	50 ns
DELAY	20 ns
AMPLITUDE	
POLARITY	N+
RANGE	10.0 V
% OF RANGE	99.95
OFFSET	OFF
GATE	OFF

Other controls should be left as in step b(2) above.

(3) Set RAMPS switch to .999 x3 V/ns. Measure 10-90% rise and fall times. WIDTH and DELAY switches may have to be adjusted to center the waveform on the screen and give a flat top on the pulse. The rise and fall times should be less than 3 ns.

(4) Set RAMPS RISE AND FALL switches to .999 V/ns. The rise and fall times should be 10.0 ns $\pm 5\%$ ± 3 ns (6.95 ns to 13.05 ns). Check other points within the range; the rise and fall times should be within the tolerance specified. It will be necessary to adjust width, delay and oscilloscope sweep to make the required measurement.

(5) Check all rise and fall ranges as in step (4) above.

f. Miscellaneous Function Verification

This procedure checks the external drive, gating pulse polarity, and pulse inversion functions.

(1) Connect the pulse generator to Model 1501A external drive input connector J105. Adjust pulse generator output amplitude to approximately +1.5 V.

(2) Set Model 1501A CLOCK switch to EXT position. Observe Model 1501A output and vary pulse generator frequency. The Model 1501A frequency should follow the pulse generator frequency.

(3) Set POLARITY to N-. The pulse should now be negative-going with the same baseline.

(4) Set POLARITY to I+. The pulse should now be inverted, with the pulsetop at the baseline and vice versa.

(5) Set CLOCK to INT. Connect pulse generator output to Model 1501A synchronous gate input connector J107. Monitor the main pulse output as well as the trigger output.

(6) Set GATE to ON. Adjust pulse generator output until amplitude exceeds +1.5 V. The Model 1501A output should be gated on for the duration of the gating signal and the trigger output should also be gated.

(7) Set GATE to OFF. The Model 1501A main output and trigger output should be gated off during the gate pulse.

(8) Connect pulse generator output to asynchronous gate input connector J106. Monitor main pulse output and trigger output.

(9) In both gate on and gate off operation, the main pulse output should be gated, but the trigger output should run continuously. This completes performance verification.

4-4 RECALIBRATION PROCEDURE

a. General

The recalibration procedure should be performed only when components are replaced or when the instrument fails to meet specifications. Recalibration should not be performed on a routine basis.

b. Recommended Test Equipment

The test equipment required for recalibration is the same as that required for performance verification.

c. Procedure

WARNING

When top and bottom covers are removed, hazardous voltages are exposed when primary power is connected. Use caution when working near the Power Transformer or AC Power Input.

(1) Turn Model 1501A off and disconnect primary power. Remove top and bottom covers.

(2) Set Model 1501A on its bottom and reconnect primary power. Turn instrument on and allow a 10-15 minute warmup period.

(3) Connect the digital voltmeter between ground test point and +15 V test point. Check that the voltage is +15 V $\pm$ 150 mV.

(4) Connect the digital voltmeter high side probe to the -15 V test point. Check that the voltage is -15 V $\pm$ 150 mV. If either 15 V supply is out of tolerance, R11 in the -15 V supply and R28 in the +15 V supply must be padded with 1% metal film resistors to bring the supplies into tolerance.

(5) Connect the digital voltmeter high side probe to the +5 V test point. The voltage should be +5 V $\pm$ 0.5 V.

(6) Connect the digital voltmeter between ground test point and frequency test point. Set FREQUENCY vernier switches to 0000 (range unimportant) and adjust R27 on the frequency D/A board for a reading of less than 5 mV on the digital voltmeter.

(7) Set FREQUENCY vernier switches to 4995 and adjust R30 on the frequency D/A board for a reading of 4.995 V $\pm$ 10 mV.

(8) Repeat steps (6) and (7) until no further adjustment is necessary.

(9) Repeat the procedure for delay, width, leading, trailing, amplitude, and offset D/A converters. Use 000 and maximum front-panel switch settings for adjustment, except for amplitude, which has a minimum setting of 5000. In this case the minimum setting should result in a voltage reading of less than 1 mV.

(10) Set FREQUENCY to 25.0 MHz. Connect the trigger output to frequency counter input. Set WIDTH and DELAY to 10 ns. Other control settings should be as follows:

CLOCK INT
GATE OFF
PULSE MODE SINGLE
OFFSET OFF
AMPLITUDE N+, 2.50 V, 50.00%

(11) Adjust R68 on the clock board for a frequency reading of 25.0 MHz $\pm 2\%$ (25.6 to 24.5 MHz).

(12) Set FREQUENCY to 49.95 MHz. Adjust R53 on the clock board for a frequency reading of 49.95 MHz $\pm 2\%$ (50.95 to 48.95 MHz).

(13) Set FREQUENCY to 5.00 MHz. Adjust R26 on the clock board for a frequency reading of 5.00 MHz $\pm 2\%$ (5.1 to 4.9 MHz).

(14) Repeat steps 11-13 until low, middle, and high frequencies all fall within the required tolerance.

NOTE

It is to the user's advantage to calibrate the instrument as closely as possible. The 5-50 MHz frequency range is controlled by analog circuits; the other ranges are divided digitally from this range.

(15) Turn off primary power and mount the delay and width board on an extender. Turn on primary power.

(16) Connect the output of the Model 1501A to the input of the digital readout oscilloscope. Connect the Model 1501A trigger output to the oscilloscope trigger input.

(17) Set controls as follows:

DELAY 50ns

FREQUENCY 50kHz

All other controls should be left as specified in step (10) above.

(18) Set WIDTH to 1 μ s on the 1-10 μ s range. Adjust R60 on the width and delay board for a pulse width of 1 μ s $\pm 2\%$ (1.02 to .98 μ s).

(19) Set WIDTH to 9.99 μ s on the 1-10 μ s range. Adjust R46 for a pulse width of 10 μ s $\pm 2\%$ (10.2 to 9.8 μ s).

(20) Repeat steps 18 and 19 until no further adjustment is necessary.

(21) Set WIDTH to 10 ns. Adjust R185 for a pulse width of 10 ns $\pm 2\%$ (10.2 to 9.8 ns).

NOTE

In the above steps and following steps, it is desirable to calibrate to better than 5% accuracy to allow for temperature drift and component aging.

(22) Set WIDTH to 10.0 μ s on the 10-100 μ s range and adjust R179 for a pulse width of 10.0 μ s $\pm 2\%$ (10.2 to 9.8 μ s).

(23) Set WIDTH to 99.9 μ s on the 10-100 μ s range and adjust R52 for a pulse width of 99.9 μ s $\pm 2\%$ (102 to 98 μ s).

(24) Repeat steps 22 and 23 until no further adjustment is required.

NOTE

Adjustment of R46 and R60 affects all ranges. Adjustment of R60 and R179 affects ranges 3, 5, and 7 only. Adjustment of R185 affects range 0 only.

(25) Check ranges 1, 2, 4, and 6 for error. Trimmers R46 and R60 may be readjusted to balance error on those ranges.

(26) Check ranges 3, 5, and 7 for error. Trimmers R60 and R179 may be readjusted to balance error on those ranges.

(27) Check range 0 and readjust R185 if necessary.

(28) Set PULSE MODE to DOUBLE and WIDTH TO 10.0 ns.

(29) Repeat steps 18-27 for the delay circuit, using the DELAY control wherever WIDTH is specified, and measuring the delay from the 50% point on the trailing edge of the first pulse to the 50% point on the trailing edge of the second pulse. The adjustments for delay are listed below.

NOTE

The adjustment in Step 21 is made with double pulse off and measuring from the leading edge of the T_0 output to the leading edge of the output pulse.

Step 18	-	R17
Step 19	-	R21
Step 21	-	R138
Step 22	-	R136
Step 23	-	R26
Step 25	-	R17, R21
Step 26	-	R26, R136
Step 27	-	R138

NOTE

Adjustment of R17 and R21 affects all ranges. Adjustment of R26 and R136 affects ranges 3, 5, and 7 only. Adjustment of R138 affects range 0 only.

(30) The next steps in the procedure calibrate pulse amplitude, and adjust two circuits on the power supply board using trimmers mounted on the output board. Voltages are measured with respect to the floating ground on the output board (not chassis ground). Floating ground is on pins B-T and B-16, -20 V is on pins A-S and A-15, and -35 V is on pins A-R and A-14. Adjust R201 so that the -20 V supply output is $-20\text{ V} \pm 100\text{ mV}$. Adjust R204 so that the -35 V supply is $-35\text{ V} \pm 100\text{ mV}$.

(31) Set controls as follows:

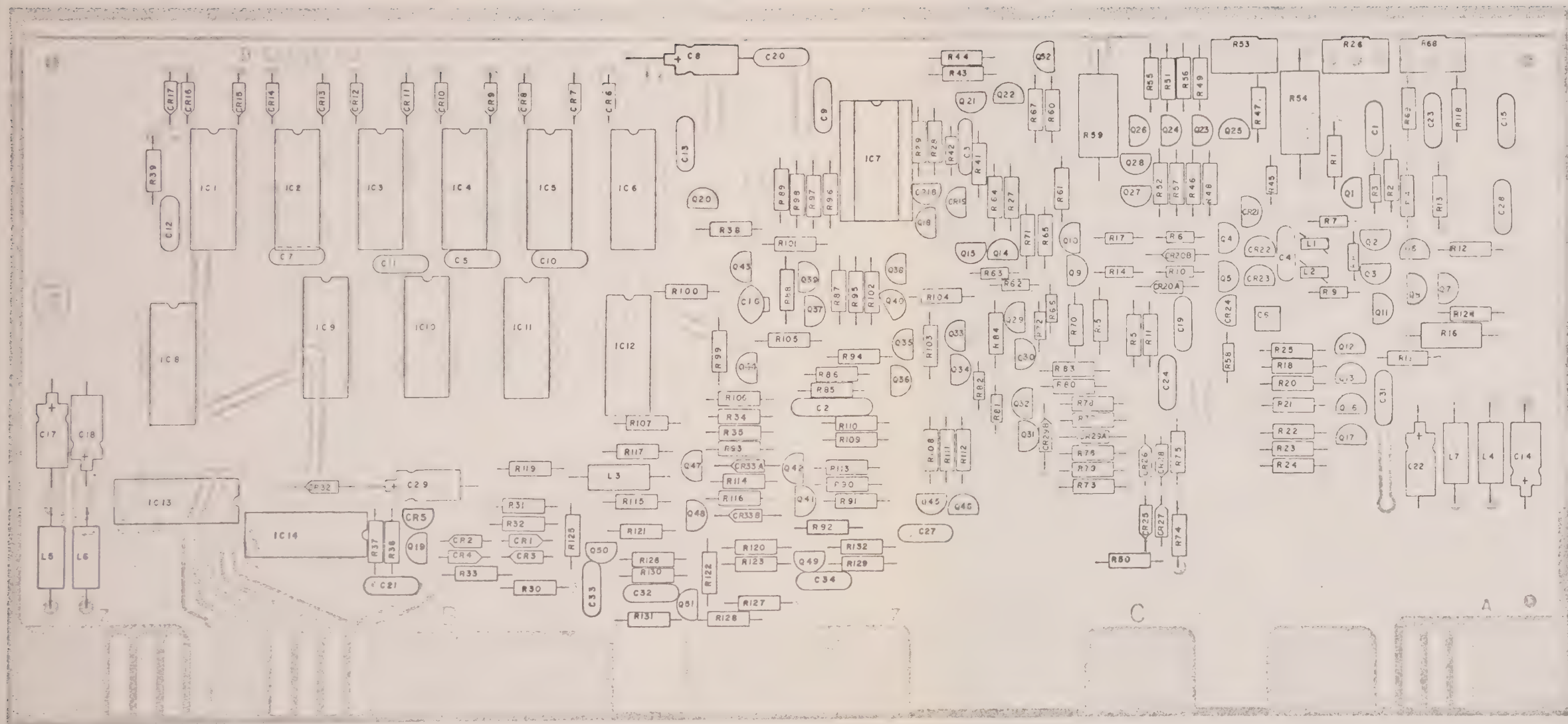
PULSE MODE		SINGLE
FREQUENCY		10 kHz
DEL		200 ns
WIDTH		500 ns
AMPLITUDE		N+, 10.0V, 50.00%

(32) Measure the voltage across R20 on the output board. Record this measurement.

1000

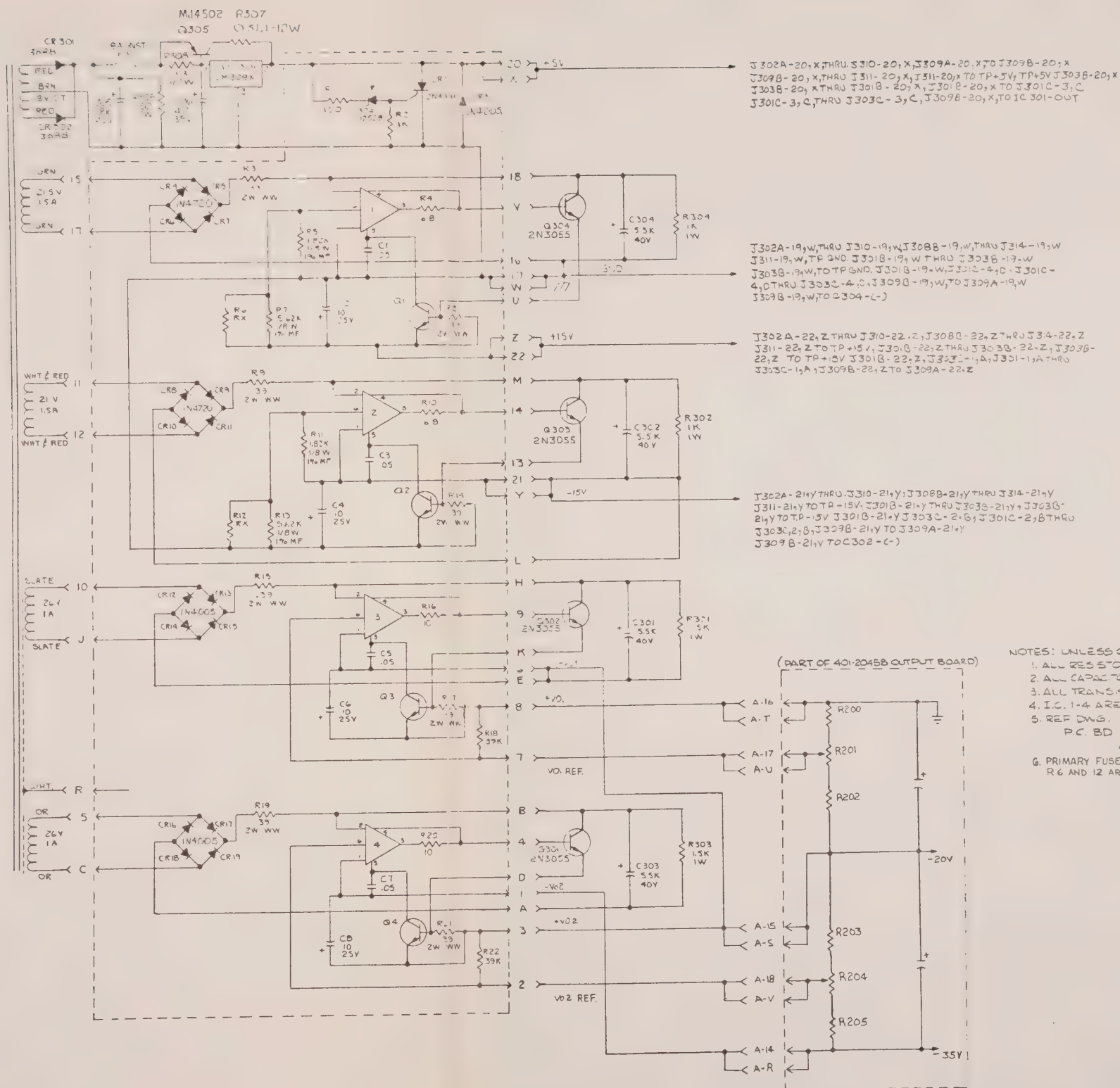
Am





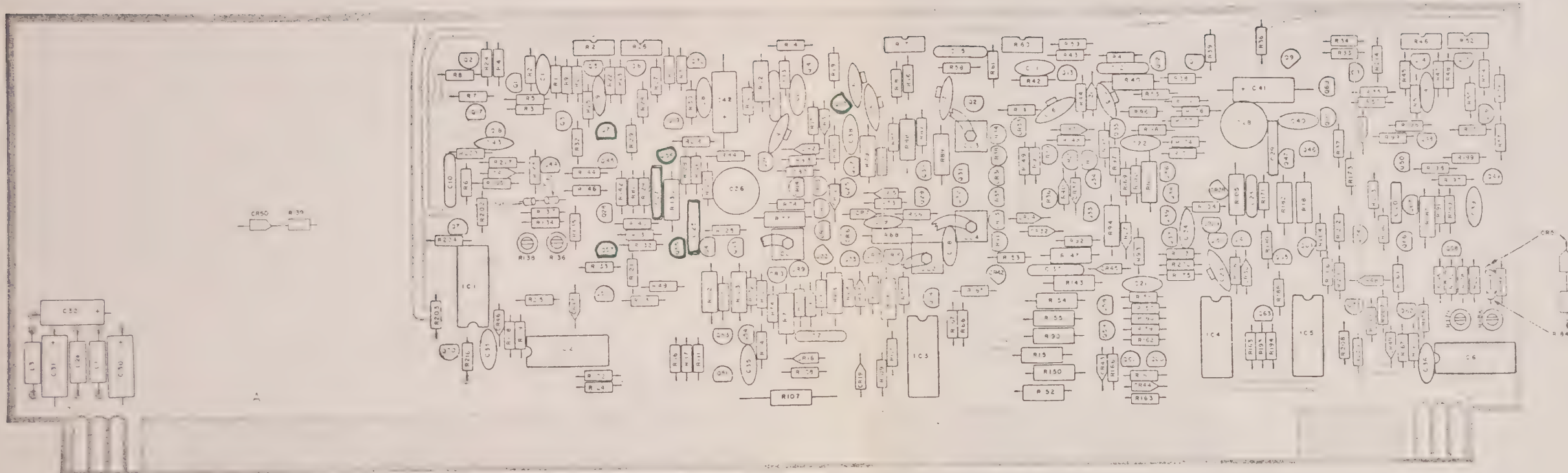
ASSEMBLY DRAWING
CLOCK BOARD

STANDARD
AC WIRING
146-21048



- NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS, 1/4W 5%.
 2. ALL CAPACITORS ARE μ F.
 3. ALL TRANSISTORS ARE 2N3004.
 4. I.C. 1-4 ARE MFC 6030.
 5. REF. DWG.
 6. PRIMARY FUSE RATING IS 2 1/2 AMP @ 117 VAC.
 7. R6 AND 12 ARE 1% MF.

SCHEMATIC:
POWER SUPPLY



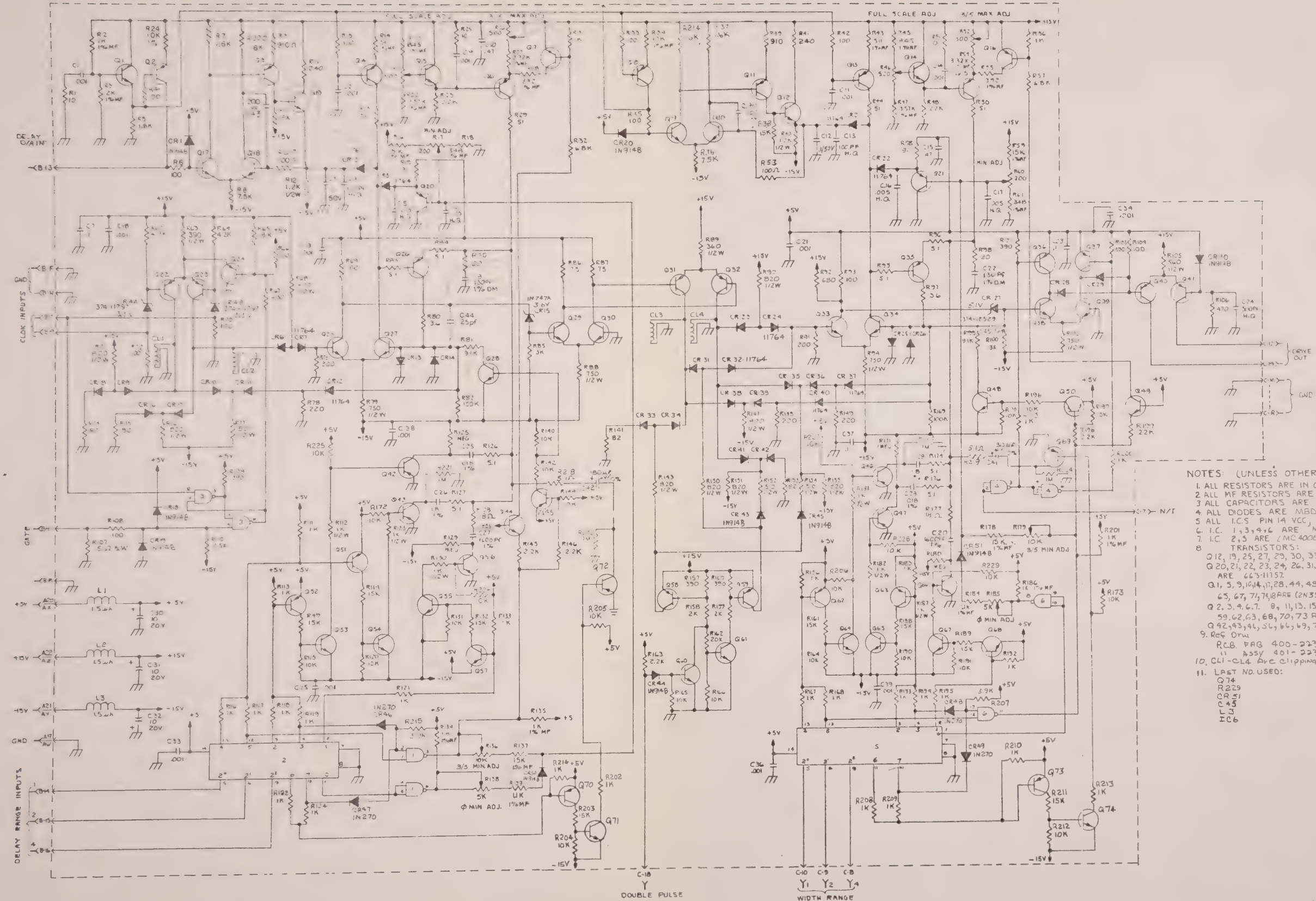
ASS'Y. DWG.
DELAY & WIDTH BOARD

MODEL NO: 1501- A

D- 401-22373

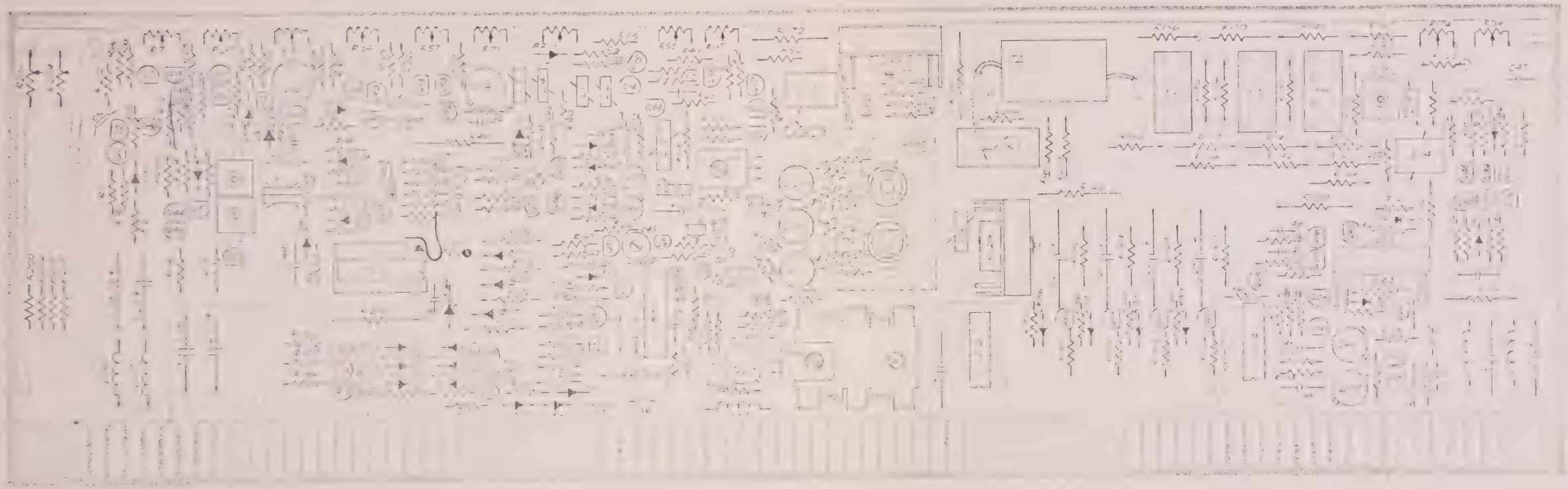
B

C-6 WIDTH D/A IN



- NOTES: (UNLESS OTHERWISE NOTED)
- 1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%, CARBON
 - 2. ALL MF RESISTORS ARE 1/8 W
 - 3. ALL CAPACITORS ARE MFD-101
 - 4. ALL DIODES ARE MBD-101
 - 5. ALL I.C.S. PIN 14 VCC, PIN 7 GND.
 - 6. I.C. 1, 3, 4, 6 ARE MC 3004P.
 - 7. I.C. 2, 5 ARE MC 4006PJ
 - 8. TRANSISTORS:
 - Q12, 19, 25, 27, 29, 30, 33, 34, 38, 39 ARE MPS-2369
 - Q20, 21, 22, 23, 24, 26, 31, 32, 35, 36, 37, 40, 41 ARE 663-11157
 - Q1, 5, 9, 10, 11, 28, 44, 49, 53, 54, 55, 60, 61, 64, 65, 67, 74, 78 ARE (2N3904)
 - Q2, 3, 4, 6, 7, 8, 11, 13, 15, 16, 45, 50, 51, 52, 57, 58, 59, 62, 63, 68, 70, 73 ARE (2N3906)
 - Q42, 43, 46, 56, 66, 69, 72, 47 ARE (2N4403)
 - 9. R25 Dnm
 - 10. RCB. FAB 400-22372
 - 11.assy 401-22373
 - 12. CL1-CL4 ARE clipping lines
 - 13. LAST NO. USED:
 - Q74
 - R229
 - CR51
 - C45
 - L3
 - IC6

SCHEMATIC,
DELAY & WIDTH BOARD



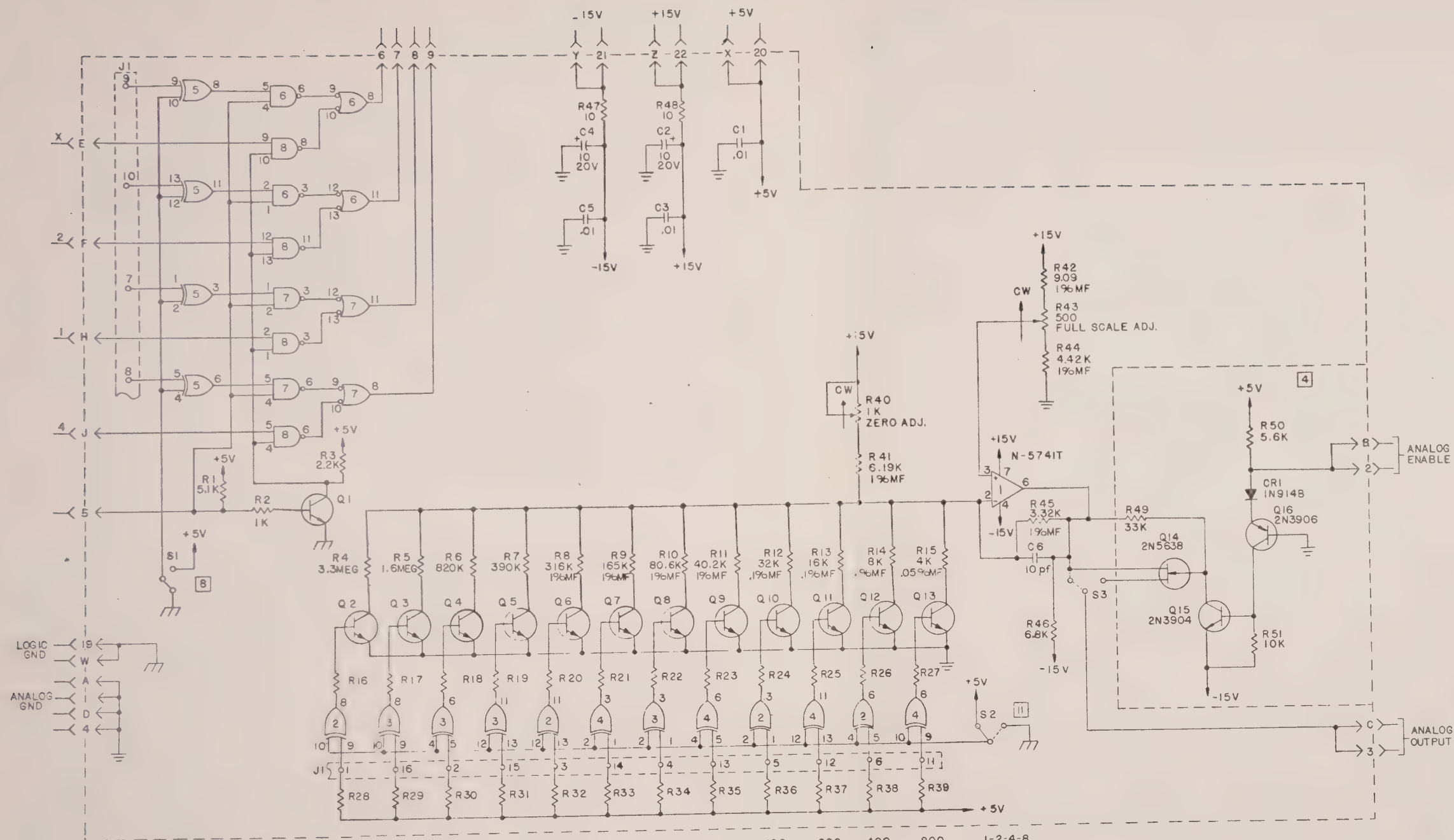
ASSEMBLY DRAWING
TYPE 'C' OUTPUT BOARD
501



ASSEMBLY DRAWING
TYPE 'C' OUTPUT BOARD

401-20458 B

SHEET NO. 2 OF 2



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS IN OHMS, 1/4W, 5%

2. R16-R39 ARE 2.2K

3. ALL CAPACITORS IN μ F

4. CIRCUITRY IN DOTTED LINES USED ON SPECIAL BOARDS ONLY

5. Q1-Q13 ARE 2N3904

6. IC 2,3,4,5 ARE MC3021P

7. IC 6,7,8 ARE MC3000P

8. ON POS. TRUE LOGIC, TIE TO +5V; ON NEG. TRUE LOGIC, TIE TO GND (H)

9. IC 2-8 PIN 14 TO +5V, PIN 7 TO GND (H)

10. REF. DWGS.

P.C.B. FAB. 400-21209

ASSY 401-21212

11. ON POS. TRUE LOGIC, TIE TO GND (H); ON NEG. TRUE LOGIC, TIE TO +5V

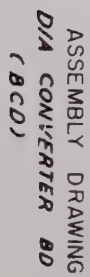
SCHEMATIC PARALLEL
D/A CONVERTER BOARD
BCD

1501A

140-

21213

B



APPENDIX A

OPTION 01 AON ASCII PROGRAMMING

A-1 INTRODUCTION

The ASCII programming option is designed to operate in a party-line data transfer bus. The address and data, both to and from the Model 1501A, are transmitted over the same seven lines (eight lines with parity check). The code used is standard ASCII alphanumeric.

When desired, each character can be checked for even parity. When a parity error is detected, an error signal is generated by the Model 1501A and the character having the parity error is inhibited from entry into the internal storage registers. When data is read from the Model 1501A, even parity is generated, character by character, and the proper parity bit is present on the eighth ASCII data line.

When reading program data from the Model 1501A, the clock may be supplied externally, or an internal clock may be selected by a jumper on one of the internal programming circuit boards.

The ASCII programming option can be operated with the E-H Model 1012 Keyboard, provided external +5 V power is supplied, and the clock output is shifted from pin 20 to pin 18 on the programming connector.

A-2 PROGRAMMING FORMAT

a. **Address.** There are two basic address requirements; unique instrument address, and function address within the instrument. The instrument must be addressed before any programming or interrogation of the unit can be done. The address consists of three characters, alpha or numeric, and are selected by jumpers on the internal address board. Unless otherwise specified, the instruments are factory-wired with an address "PG1." If desired, this can be changed by changing the jumpers on the address board. For example, if "PG2" is desired, the connection at IC11 pin 2 should be moved from the A1 line to the A2 line. Once the address characters have been entered, the instrument functions are available for programming or readout. The instrument address, once entered, remains valid until a period "." is entered. At this point no further programming or program readout can be done until the instrument is once again addressed.

Once the instrument address has entered, a single alpha character selects a function such as frequency, delay, amplitude, offset, etc. These function characters are listed in Table A-1. The next five numeric characters following the function address are stored as data for the function. The sequence and definition of the five data characters are also shown in Table A-1.

b. **Stored Data Readout.** Stored program data may be read out, one complete function at a time, by first addressing the instrument, then selecting the function with a single alpha character. The next character following the function character must be a question mark "?". When the "?" has

been clocked in, the first data character will be present on the data input/output lines. There must be five clock pulses sent to the instrument for a complete readout of the five data characters. Once a readout is initiated, all five characters must be clocked out. A period will not reset the box address once a readout has initiated. Characters are read out in the same sequence as written (see Table A-1).

c. **Data Reset.** When primary power is applied to the Model 1501A (turning on the POWER switch), all internal storage registers are reset to "0" automatically. This means that initially all functions must be programmed. After a function is programmed in the initial process after power turn-on, it can be edited independently. In operation, complete data reset can occur in two ways.

1. **C0.** This reset mode is used in the following manner: The instrument address is entered on the data lines, followed by "C0". This resets all function storage registers to zero, but does not reset the instrument address.

2. **EXTERNAL RESET (GOMR).** This is a single external control line which, when activated, resets all functions as well as the instrument address. This line is brought out to pin 22 of rear-panel connector J109.

In the reset state, functions are programmed as follows: maximum attenuation, inverted pulse mode, negative pulse, zero offset, Gate Off mode, frequency, delay, width, rise and fall times at minimum, internal clock, and single pulse.

A-3 DATA FORMAT

Referring to Table A-1, the Function column lists the seven functions together with their proper alpha characters. The first character following the function character is mode control character. For example, the mode control character for frequency selects either internal or external clock by entry of a "0" or "1", respectively. Only the least significant bit of the character is stored, so that any even number will be recognized as a "0" and any odd number will be recognized as a "1".

The mode characters for "T", positive ramp, and "O", offset are not used and may be any numeric character. There must, however, be a character entered (usually zero) when the function is programmed.

Following the mode character is a range character, selected by referring to Table A-1. In the case of offset, a 2 selects positive offset and a 4 selects negative offset. The "T" (positive ramp) function does not use a range character, but the position must be filled with numeric character, as in the "T" and "O" mode functions described previously.

The third, fourth, and fifth characters following the function character are vernier characters for fine programming of the function within the range programmed.

It should be noted that even though all character positions must be filled in the initial programming, when a function is edited only those characters up to and including the character to be edited need to be programmed.

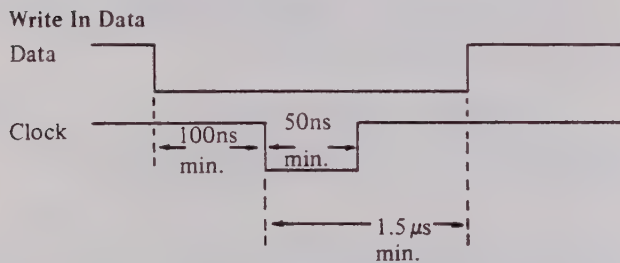
When using the Model 1501A with a paper tape reader or other data source using a "rubout" character to correct errors, the "rubout" will be ignored and not counted as a character. If using the Model 1501A in a party-line bus with other instruments such as the Model AMC 1000 Waveform Analyzer or the Model AMC 4001 Power Supply, the rubout character cannot be used in the program for these units:

A-4 INPUT REQUIREMENTS

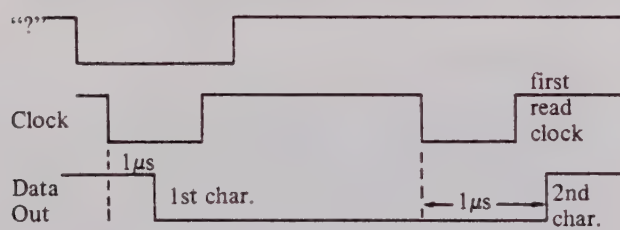
a. Data Input. The ASCII programming option is compatible with TTL logic levels, and is normally supplied with ground true logic. High true, greater than +2.5 V, can be selected by an internal jumper. Each programming input is a standard TTL load. High level input is +5.0 V maximum.

b. Data Output. The data output is from open collector devices capable of sinking 300 mA. True level is normally ground. Positive true is selected by an internal jumper.

c. Strobe (Clock) Timing is shown below:

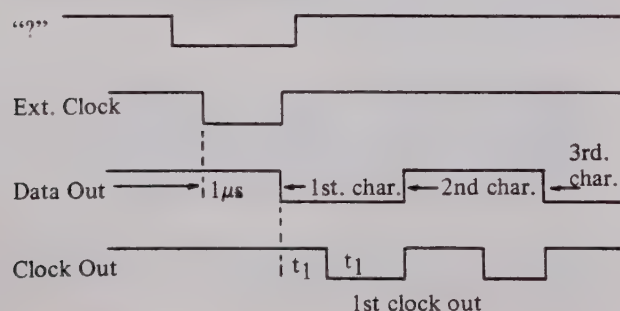


Read Out Data - External Clock



The first data character is valid 1µs after the “?” clock is received, and remains valid until 1µs after the next clock pulse is received.

Read Out Data - Internal Clock



The first data character is valid 1µs after the external data clock. The internally-generated clock is a square wave, and the data out changes at the trailing edge of the clock pulse. The first clock out occurs at one-half the clock period. The internal clock frequency may be adjusted internally by changing the value of R26 and C4 on schematic diagram 140-22315. The maximum clock frequency is 500 kHz. The clock is normally shipped with a clock frequency of approximately 1.4 kHz (700µs period). In this case, the first clock occurs about 350µs after the “?” character is clocked in.

A-5 VERNIER PROGRAMMING

a. Frequency. The basic ranges change in decades, beginning with 0.5 Hz and ending with 50 MHz. Because of the “5” relationship of the ranges and the “10” relationship of the vernier programming, a calculation must be made to determine the proper three-digit vernier program. To find the proper three-digit vernier, multiply the required frequency by two and take the three most significant digits as the vernier program. For example, if the required frequency is 260 kHz, the required program on the 50 kHz-500 kHz is 2 x 260, or 520. On the lower ranges, the frequency should be converted into Hz before multiplying (e.g., 1.87 kHz to 1870 Hz.).

b. Delay/Width. The delay and width vernier programming is straightforward, with a vernier program of 100 corresponding to the low end of the range and a program of 999 corresponding to the high end of the range. For example, a width or delay of 250 ns is programmed as 250 on the 100 ns-1 µs range.

c. Amplitude Programming. The basic (unattenuated) amplitude range is 5 V with 000 vernier and 9.99 V with 999 vernier. To determine the vernier for a given amplitude, including attenuation, use the formula below:

$$\text{Ampl. Vernier} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005}$$

d. Offset Programming. The range of offset programming is from 0 to 5V. The vernier program is the required offset value in volts, multiplied by 200. For example if the required offset is 200 mV, the vernier is 200 x 0.2, or 040.

d. Leading and Trailing Edge Ramps. Since the leading and trailing edge ramps of the Model 1501A are constant slope with respect to changes in amplitude vernier, and constant risetime with respect to changes in attenuation, a calculation must be made to determine the program for a given combination of amplitude and rise/fall time. The *fastest* leading and trailing edge times are obtained at a vernier of 999, and the *slowest* times at a vernier of 100. To determine the proper vernier, use the following formula:

$$\text{Ramp Rate} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{rise or fall time}}$$

where “K” = .8 for 10-90%, K = .6 for 20-80%, etc.

SAMPLE PROGRAM

Required Amplitude: 800 mV

Required 10-90% risetime: 20 ns

Step 1. Determine attenuation value by inspecting Table A-1. An 800 mV output will be obtained on Range 4 which has an attenuation value of 8.

Step 2. Set attenuator to Range 4.

Step 3. Determine amplitude vernier setting using the attenuation value found in Step 1.

$$\begin{aligned} \text{Ampl. Vernier} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005} \\ &= \frac{(.800) \times (8) - 5}{.005} \\ &= 280 \end{aligned}$$

Step 4. Set Amplitude vernier to 280.

Step 5. Determine ramp rate using:

$$\begin{aligned} \text{Ramp Rate} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{risetime}} \\ &= \frac{(.800) \times (8) \cdot 8}{20 \text{ ns}} \\ &= \frac{5.12 \text{ V}}{20 \text{ ns}} \\ &= \frac{5.12 \text{ V}}{.02 \mu\text{s}} \\ &= 256 \text{ V}/\mu\text{s} \end{aligned}$$

By inspecting Table A-1, we find that a ramp rate of 256 V/μs can be obtained with Ramp Range = 1.

Step 6. Set Ramp Range to 1.

Step 7. Set Ramp vernier to 256.

NOTE

Since the vernier only varies between counts of 100 to 999, it may be necessary to multiply the Ramp Rate by either 10 or 100 to obtain the three-digit vernier setting. Example: if Ramp Rate = 24 V/μs, then Vernier = 24 x 10 = 240. Example: if Ramp Rate = 1.3 V/μs, then Vernier = 1.3 x 100 = 130.

A-6 ASCII CIRCUIT DESCRIPTION

a. **Block Diagram Level.** (See Figure A-1) The block diagram contains the major functions performed along with the IC numbers which make up the logic. The diagram is divided by a dotted line showing which parts of the logic are

located on each of the two cards. Basically, card B provides the box address and function decoding, and card A directs the data characters to their correct storage registers.

Eight Data Lines and a Clock Line are brought in to the Data Input Polarity Select logic. The input true state is selected here, so that the seven data lines to the Input Data Decode logic are always high-level true. If connected, the input character is checked for even parity, and an error signal generated when a parity error is detected. The parity error can also be connected to inhibit clocking that character in.

The Box Address Sequence Control insures that the three characters which have been selected as the box address have been sent in the proper order, before the interface will respond to a write or read instruction.

The Function Decode is armed by the valid box address and stores a function address. The output from the Function Decode is seven lines, one to each of the seven function storage registers. The alpha character "C" is also stored by the Function Decode.

Once a Function has been decoded the next five characters must be numerics. Any other character will reset the Function Decode.

The Input/Output Character Counter counts the five characters and addresses the storage registers on the D/A cards.

The Data Input Control takes the least significant bit of the first character and temporarily stores it. When the second character is strobed in, its most significant bit is replaced with the first character's LSB. The third, fourth and fifth characters are stored as full 4-bit characters. There are thus actually four characters clocked into the D/A storage registers.

The Data Output Control gates the MSB of the first and second characters (stored as one 4-bit character) to the LSB on the data lines to be read as the first character out. The other three bits are then gated to the output as the second character. Each of the other three BCD characters is then clocked out in sequence.

b. **Card B.** (See schematic D140-22318). The input to the ASCII interface is through J1 on Card B. This connector is located in the upper right hand corner of the board. The clock line is also brought in thru this connector.

The inputs each have provision for a pull-up resistor to +5 volts. These are normally only used when the 1501A is the last instrument on the data bus.

IC-24,25 and 1 gate in IC16 are exclusive NOR gates. When their inputs are at the same logic level, their output is high, which is the true state for data at their output. The common line which is connected to one input of each of the input gates, is tied to ground for low-true logic input, or to +5 volts for high-true logic. This is done with a single wire as indicated by S1.

IC-22 is an 8-Bit Parity Tree. Its output, pin 8, is high as long as three is an even number of its inputs high. If the output of IC-16, pin 8, is connected to pin 4 of IC-4, via S3, then a non-even parity character inhibits the clock one-shot, IC-4, from strobing that character. For even-parity error output

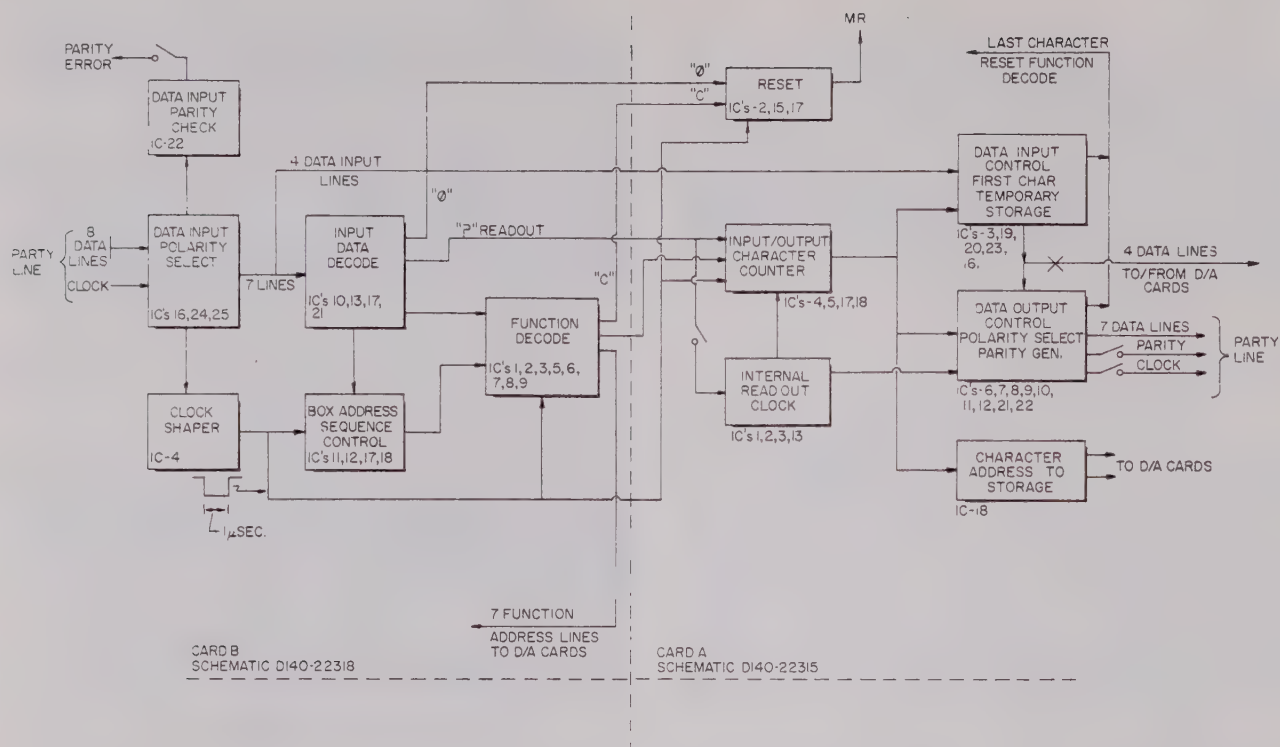


Figure A-1 1501A ASCII Interface Block Diagram

signal, IC-16, pin 8 is connected to IC-15, pins 6 and 7, via S2. The output from IC-22, pin 6, is for odd parity checking.

The rub-out detector is IC-23. If all its inputs are high, its output, pin 8, is low and inhibits the clock one-shot, IC-4 from strobing that character.

The 3 least significant bits are decoded to 1-of-8 by IC-10. The next 2 bits, 4 and 5, are decoded to 1-of-4 by IC-17, output pins 1,2,3, and 4. These lines are designated A0 thru A7, and B0 thru B3. Two of these lines are connected to the box address gates of IC11 and IC-12 via jumper wires to define the box address. The schematic shows the connections for box address PG1.

Input data bits 5,6, and 7 are decoded by IC-21, to determine whether a character is alpha or numeric. These outputs are used as part of the box address decoding and also the function decoding.

(1) Box Address Sequence Control. Initially, the binaries of IC-18 are in a reset state. Output pin 12 of IC-17 will be low. If a "P" is decoded, pin 6, IC-12, will go high, forcing pin 8, IC-12 low. This allows the clock on pin 9, IC-19, to advance the sequence counter, IC-18. Output pin 13, IC-17 will then be low. If the next character is not a "G", then the clock on pin 4, IC-20, will reset the sequence counter. If the proper three characters are received, then pin 15, IC-17, will go low, indicating the box has been addressed, and will inhibit any further clocks from resetting the sequence counter; via pin 5, IC-20.

Pin 3, IC-1 will now be low which will allow the next alpha character, decoded via IC's 1,2, and 3, the Function decode, to be strobed into the proper Flip-flop of IC 8, or 9. When a

Function has been selected, the output of IC-7, pin 8, inhibits any more clocks to the Function Flip-flops. If the next character is not a numeric, the Function Flip-flop is reset by the output from IC-20, pin 8.

If the 5 characters following the Function alpha character are all numeric, the Function Flip-flop is reset after the fifth character by the Last Digit reset signal on pin B17 of the P.C. connector.

(2) Clock Timing. All internal clocking is derived from the clock one-shot, IC-4, pin 6. Data to the internal storage registers is strobed in on the leading, or negative-going edge of IC-4, pin 6. The box address and the Function characters are strobed at the trailing edge. The characters must therefore be valid at the time of the external clock and remain valid for the width of the one-shot. The one-shot is normally set for approximately 1 μ sec, but may be changed by changing the RC time constant circuit of R11 and C8.

c. Card A. (See schematic D1140-22315)

(1) Writing in Data. The initial state of the character counter, IC-5 and one-half of IC 4, is set when the Function Selected line on pin B18 of the P.C. connector is low. When a function has been addressed, this line goes high at the trailing edge of the clock. This enables the input decoder IC-19, via pin 7. Pin 5 of IC-19 will then go low. Pin 11, IC-19, will be high, forcing the clock input of IC 3, pin 3, low. This is the first character, LSB, temporary storage. At the trailing edge of the next character clock, the character counter is advanced and pin 11 of IC-19 goes low which clocks the LSB into IC-3, pin 2. Pin 11, IC-20 also goes high, enabling the input gates for the 3 least significant bits. This line also goes to Card B,

via pin B14, where it enables the next four clocks to strobe data into the storage registers.

When the next clock arrives, bits 1,2, and 3 are present at the outputs, pins 3,11, and 8 of IC-23. The temporarily stored first character's LSB is present at pin 11, IC-16, as it is stored along with the other bits on the leading edge of the second character clock.

On the trailing edge of the second character clock, the character counter is again advanced and pin 12, IC-19 goes low which enables the MSB of the data via IC-23, pin 4, and also holds the output of IC 20, pin 11 high.

At the trailing edge of the fifth data clock, the character counter is advanced and IC-19, pin 3 goes low, resetting the Function Decode Flip-flop. The Function Selected line goes low, re-initializing the character counter and disabling the input decode control, IC-19. The output from IC-19, pin 7, is therefore a negative-going spike generated at the trailing edge of the character clock.

(2) Reading out Data. Read out is initiated by a “?” mark immediately following a Function character. The Read Out signal on pin A2 will be high, inhibiting the Character Clock from advancing the character counter, via IC-17, pin 1. IC-19, pin 5 will be low, thus clocking the high level on IC-4, pin 2 into the Flip-flop. IC-4, pin 5 goes high enabling the Data Output decode Control, IC-6. IC-4, pin 6 goes low disabling the Data Input decode control IC-19. The first 4 bits of data from the selected function are then present at pins BK, BJ, BH and BL. The 3 LS bits are inhibited by the high output from IC 7, pin 11. The MSB on IC-8, pin 2, is gated to the output LSB. When the first of the five data clocks arrives, the data output will either be a 1 or a 0, depending on the Mode bit that is in storage.

The character counter is advanced and IC-6, pin 11 goes low, enabling the 3 least significant bits and inhibiting the MSB. The next data clock strobes only the 3 least significant bits. At its trailing edge, the character counter is advanced and IC-6 pin 12 goes low. This enables the MSB to be present on the data bus. The character counter is decoded by IC-18, pins 8 and 11 to address the next three characters from storage.

At the trailing edge of the fifth readout clock, IC-6 pin 3 goes low, resetting the Function Decode Flip-flop, ending the readout sequence.

During a readout sequence, data bus lines 5 and 6 are forced to be only ‘1’s, and bit 7 is forced to be a ‘0’ bit.

(3) Readout with Internal Clock. The internal clock is generated by turning on the multivibrator, IC-1, and dividing it down with Flip-flop IC 3. IC 13, pin 1 is strapped to +5 volts, at S3. IC 18, pin 1 is connected to IC 3, pin 9, which then is the clock used to step the character counter. The clock multivibrator is turned on when readout signal on IC 4, pin 2 is clocked in.

(4) Master Reset. When power is applied, Master Reset is held low by capacitor C6 being charged by the input current of IC-20, pin 4. The output from pins 6 and 8 of IC-16 reset the box address sequence counter and the Function Decode Flip-flop.

(5) “C0” Reset. “C” is decoded and stored as all other box functions. At the next character clock, a Master Reset will be generated via IC 15 pin 11, if the character is a zero. At the trailing edge of the clock, the output from IC 13, pin 11 will be a negative pulse determined by R6 and C5, which will reset the Function Decode Flip-flops.

Table A-1 ASCII Programming Format

Function	ID Character	Mode Control	Range Character	Range	Vernier Character
Frequency	F	0=Internal Clock 1=External Clock	0	0.5-4.995 Hz	100-999
			1	5-49.95 Hz	100-999
			2	50-499.5 Hz	100-999
			3	0.5-4.995 KHz	100-999
			4	5-49.95 KHz	100-999
			5	50-499.5 KHz	100-999
			6	0.5-4.995 MHz	100-999
			7	5-49.95 MHz	100-999
Delay	D	0=Single Pulse 1=Double Pulse	0	10-99.9 ns	100-999
			1	100-999 ns	100-999
			2	1-9.99 μ s	100-999
			3	10-99.9 μ s	100-999
			4	100-999 μ s	100-999
			5	1-9.99 ms	100-999
			6	10-99.9 ms	100-999
			7	100-999 ms	100-999
Width	W	0=Inverted Pulse 1=Normal Pulse	0	10-99.9 ns	100-999
			1	100-999 ns	100-999
			2	1-9.99 μ s	100-999
			3	10-99.9 μ s	100-999
			4	100-999 μ s	100-999
			5	1-9.99 ms	100-999
			6	10-99.9 ms	100-999
			7	100-999 ms	100-999
Unattenuated Ramp Slope: Leading Edge (Neg Ramp)	L	0=Gate Off 1=Gate On	0	Uncalibrated Range*	100-999
			1	0.1-0.999 V/ns	100-999
			2	10.0-99.9 V/ μ s	100-999
			3	1.0-9.99 V/ μ s	100-999
			4	0.1-0.999 V/ μ s	100-999
			5	10.0-99.9 V/ms	100-999
	T	N/A	N/A		
Attenuation and Amplitude	A	0=Negative Pulse 1=Positive Pulse	0	(x128) 40-80 mV	000-999
			1	(x64) 80-160 mV	000-999
			2	(x32) 156-312 mV	000-999
			3	(x16) 312-625 mV	000-999
			4	(x8) 0.62-1.25 V	000-999
			5	(x4) 1.25-2.5 V	000-999
			6	(x2) 2.5-5.0 V	000-999
			7	(x1) 5.0-10.0 V	000-999
Offset	O	N/A	0	No Offset	000-999
			2	0 to +5 V	000-999
			4	0 to -5 V	000-999

CO-Reset

Period "." resets instrument address

"?" following a function character initiates readout of data

"rubout" character is ignored in Model 1501A

Note

References to Neg Ramp and Pos Ramp refer to leading and trailing edges, respectively, in positive and negative normal modes. In positive and negative inverted modes, the negative ramp becomes the trailing edge and the positive ramp becomes the leading edge.

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table A-2 Program Input Connection A-6 ASCII CIRCUIT DESCRIPTION

J110 and J111 on the rear panel can be used interchangeably as input or output connectors.

Pin No.	Connection
1	ASCII Bit 1 Input/Output
2	Gnd
3	ASCII Bit 2 Input/Output
4	Gnd
5	ASCII Bit 3 Input/Output
6	Gnd
7	ASCII Bit 4 Input/Output
8	Gnd
9	ASCII Bit 5 Input/Output
10	Gnd
11	ASCII Bit 6 Input/Output
12	Gnd
13	Not used in Model 1501A
14	ASCII Bit 7 Input/Output
15	Gnd
16	ASCII Bit 8 Output (Parity Check)
17	Gnd
18	Clock Input
19	Gnd
20	Not used in Model 1501A
21	Gnd
22	Not used in Model 1501A
23	Not used in Model 1501A
24	Not used in Model 1501A
25	Gnd

Note:
Rear-panel connectors mate with Cinch DBM-25P.

ASSEMBLY NO. 350-21902DESCRIPTION MOD KIT/ASCII GND TRUE - BCD

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
	ADD	
401-22619	D/A Serial Board Assembly	J305-307 J311-314
401-22314	ASCII-A Board Assembly	J308
249-21386	Sub Panel Rear Assembly	
401-22317	ASCII-B Board Assembly	J309
	ADD TO 820-21290	
146-26044	Doc List	Prod Ref
700-00304	Connector, 25 Pin, Male	
700-00338	Slidelock Retainer	
891-00309	Cover, Connector	
	DELETE	
401-21212	Parallel D/A Board Assy	J305-307 311-314
249-21283	Sub Panel Rear Assembly	
	DELETE FROM 820-21290	
700-00034	Connector, 50 Pin Amphenol	
700-00024	Connector, 24 Pin Amphenol	

ASSEMBLY NO. 401-22314DESCRIPTION INTERFACE A ASCII BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22313	PC Board	
401-22314	Assembly Drawing	Prod Ref
140-22315	Schematic	Prod Ref
311-00009	Cap, Cerm 500pf	C5,11
311-00021	Cap, Cerm .05 μ f 75V	C4
311-00041	Cap, Cerm .1 μ f/12V	C2,3,7-9
318-00005	Cap, Tant 10 μ f 20V	C6
318-00004	Cap, Tant 27 μ f 10V	C1
335-00022	Choke, 1 μ h	L1
376-00022	Diode, 1N914B	CR1
595-00101	Resistor 100 Ω $\frac{1}{2}$ W 5%	R6,27
595-00104	Resistor 100K $\frac{1}{2}$ W 5%	R14
595-00122	Resistor 1.2K $\frac{1}{4}$ W 5%	R7-10 18-23
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R11-13, 25 15-17,24.
595-00303	Resistor 30K $\frac{1}{2}$ W 5%	R26
595-00511	Resistor 510 Ω $\frac{1}{2}$ W 5%	R3

ASSEMBLY NO. 401-22314DESCRIPTION INTERFACE A ASCII BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
665-00053	IC MC 3000P	IC 2,7,20
665-00056	IC MC 3060P	IC3-5
665-00078	IC MC 3004P	IC13,16, 18,23
665-00084	IC MC 3022P	IC9,10,24
665-00100	IC SN75453P	IC8,11,12, 14,21,22
665-00110	IC MC 3002P	IC15,17
665-00130	IC MC 8601P	IC1
665-00123	IC MC 4038P	IC6,19
450-00308	Jack, Brown	TP5
450-00309	Jack, Red	TP4
450-00310	Jack, Orange	TP2
450-00317	Jack, Black	TP1, TP3

ASSEMBLY NO. 401-22317DESCRIPTION INTERFACE B ASCII BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22316	PC Board	
401-22317	Assembly Drawing	Prod Ref
140-22318	Schematic	Prod Ref
311-00008	Cap, Cerm 150pf	C9
311-00074	Cap, Cerm .01 μ f 100V	C2-7
318-00005	Cap, Tant 10 μ f 20V	C1
335-00022	Choke 1 μ h	L1
595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R1-9
595-00183	Resistor 18K $\frac{1}{2}$ W 5%	R11
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R10,12-20
665-00140	IC SN7427N	IC1-3 13,14
665-00130	IC MC8601P	IC4
665-00078	IC MC 3004P	IC5,6
665-00090	IC SN7430N	IC7,23
665-00144	IC MC4015P	IC8,9
665-00057	IC MC 4006P	IC10
665-00148	IC SN7425N	IC11,12
665-00100	IC SN75453P	IC15
665-00084	IC MC3022P	IC16,24,25

ASSEMBLY NO. 401-22317DESCRIPTION INTERFACE B ASCII BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
665-00053	IC MC3000P	IC19
665-00114	IC MC3007P	IC20
665-00150	IC MC4008P	IC22
665-00149	IC MC4007P	IC17,21
665-00056	IC MC3060P	IC18
700-00126	Connector, 34 Pin	J1

ASSEMBLY NO. 706-21378DESCRIPTION CABLE ASSEMBLY, DUAL 34 PIN

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-21233	Paddle Board	
700-00120	Transition 34 Pin 3M 3402	
700-00121	Transition 34 Pin 3M 3414	
700-00303	Connector, 25 Pin Female	J110, 111
757-00001	Ribbon Cable, 34 Cond	

ASSEMBLY NO. 249-21386DESCRIPTION ASSEMBLY SUB-PANEL REAR

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
248-21382	Panel	
144-21384	Silkscreen	Prod Ref
700-00337	Post, Slide Lock	
706-21378	Cable Assy, Dual 34 Pin	J110, J111
140-22748	Schematic	Prod Ref

ASSEMBLY NO. 401-22619

DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

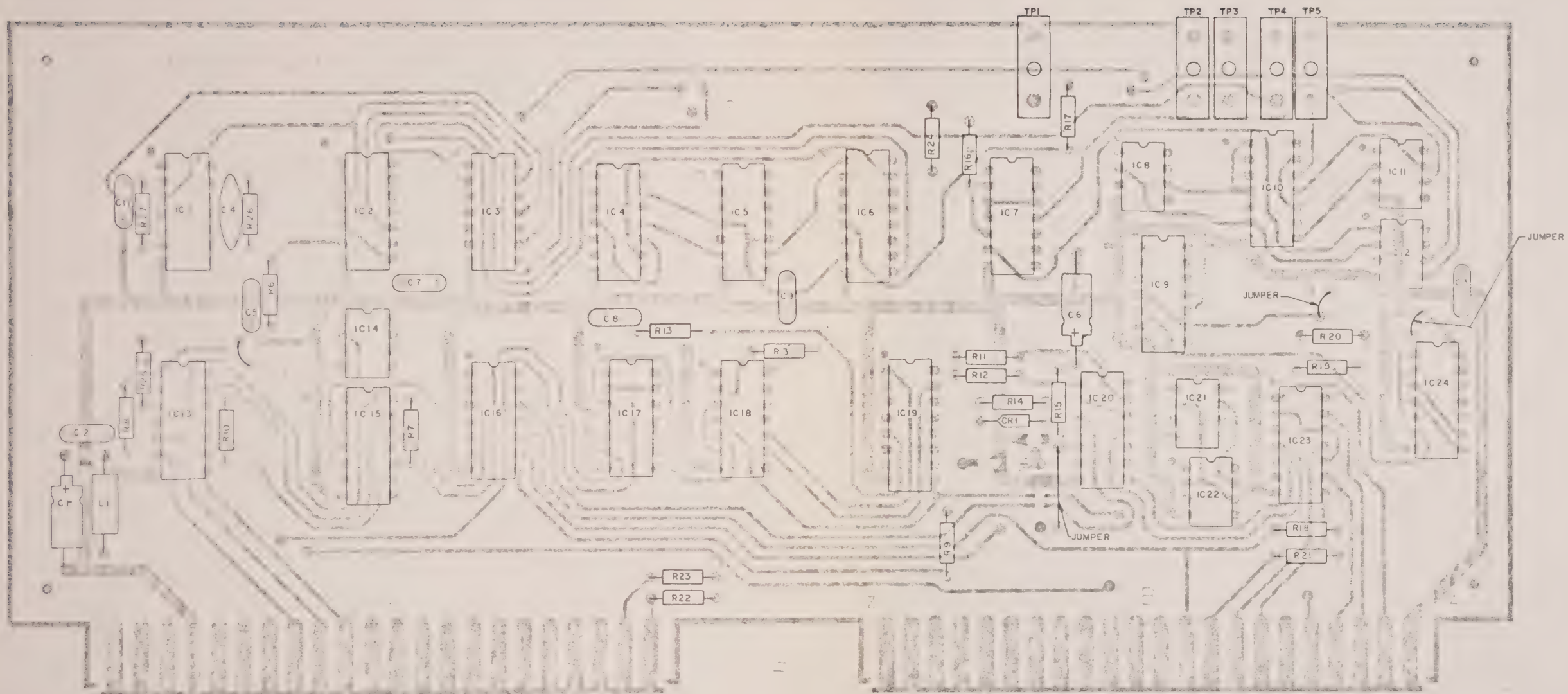
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22618	PC Board	
401-22619	Assembly Drawing	Prod Ref
140-22620	Schematic	Prod Ref
311-00001	Cap, Cerm 10pf 1KV	C3
311-00074	Cap, Cerm .01 μ f 100V	C2,5,6, 8,9
318-00004	Cap, Tant 27 μ f 10V	C1
318-00005	Cap, Tant 10 μ f 20V	C4,7
335-00022	Choke 1.0 μ h	L1
495-00054	Socket, IC 16 Pin	J1
595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R35
551-00035	Potentiometer 00 Ω 89PR	R30
551-00040	Potentiometer 1K 89PR	R27
595-00100	Resistor 10 Ω $\frac{1}{2}$ W 5%	R28,33
595-00153	Resistor 15K $\frac{1}{2}$ W 5%	R32
595-00165	Resistor 1.6M $\frac{1}{2}$ W 5%	R11
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R13-24
595-00335	Resistor 3.3M $\frac{1}{2}$ W 5%	R12
595-00394	Resistor 390K $\frac{1}{2}$ W 5%	R9
595-00512	Resistor 5.1K $\frac{1}{2}$ W 5%	R34

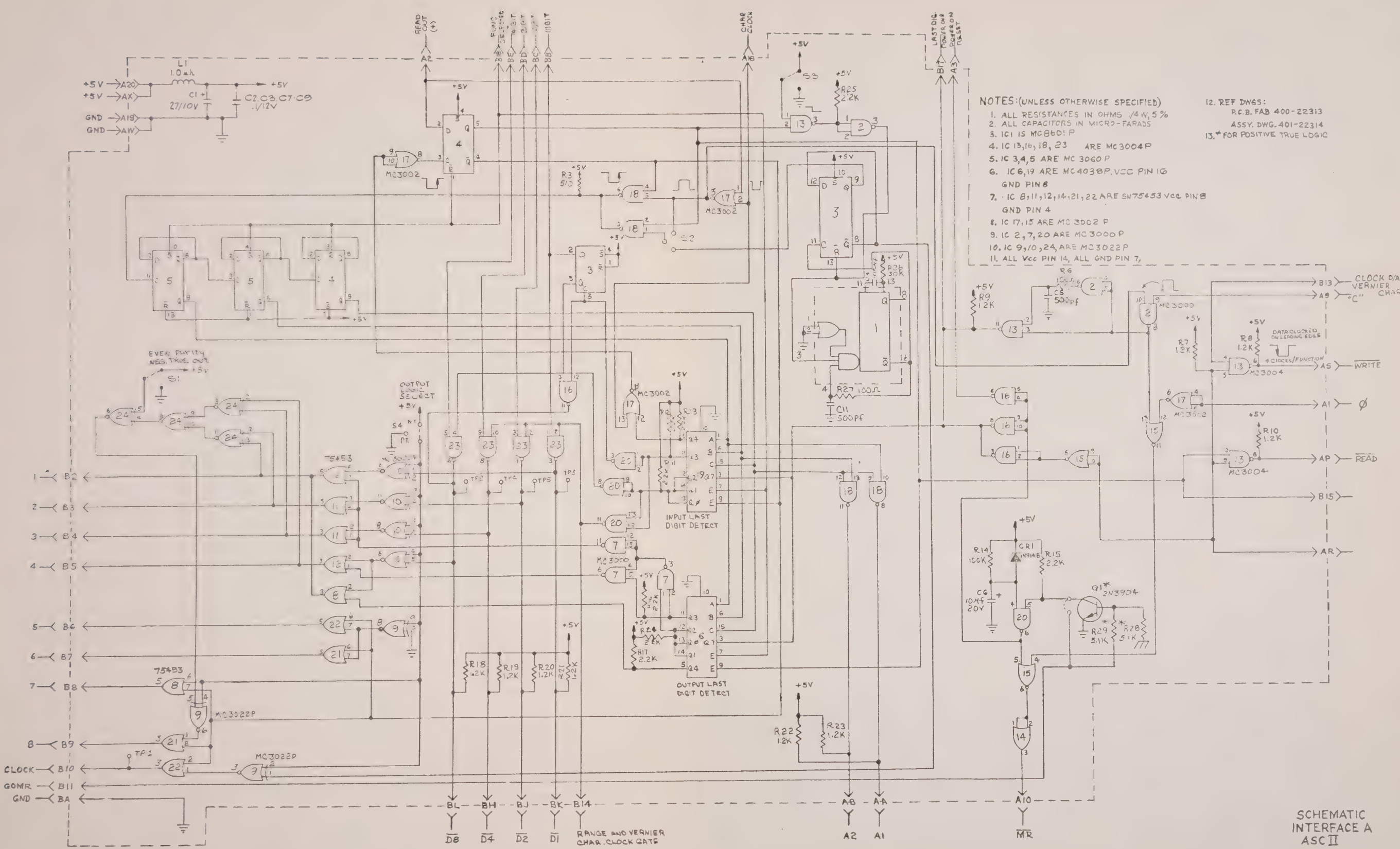
ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

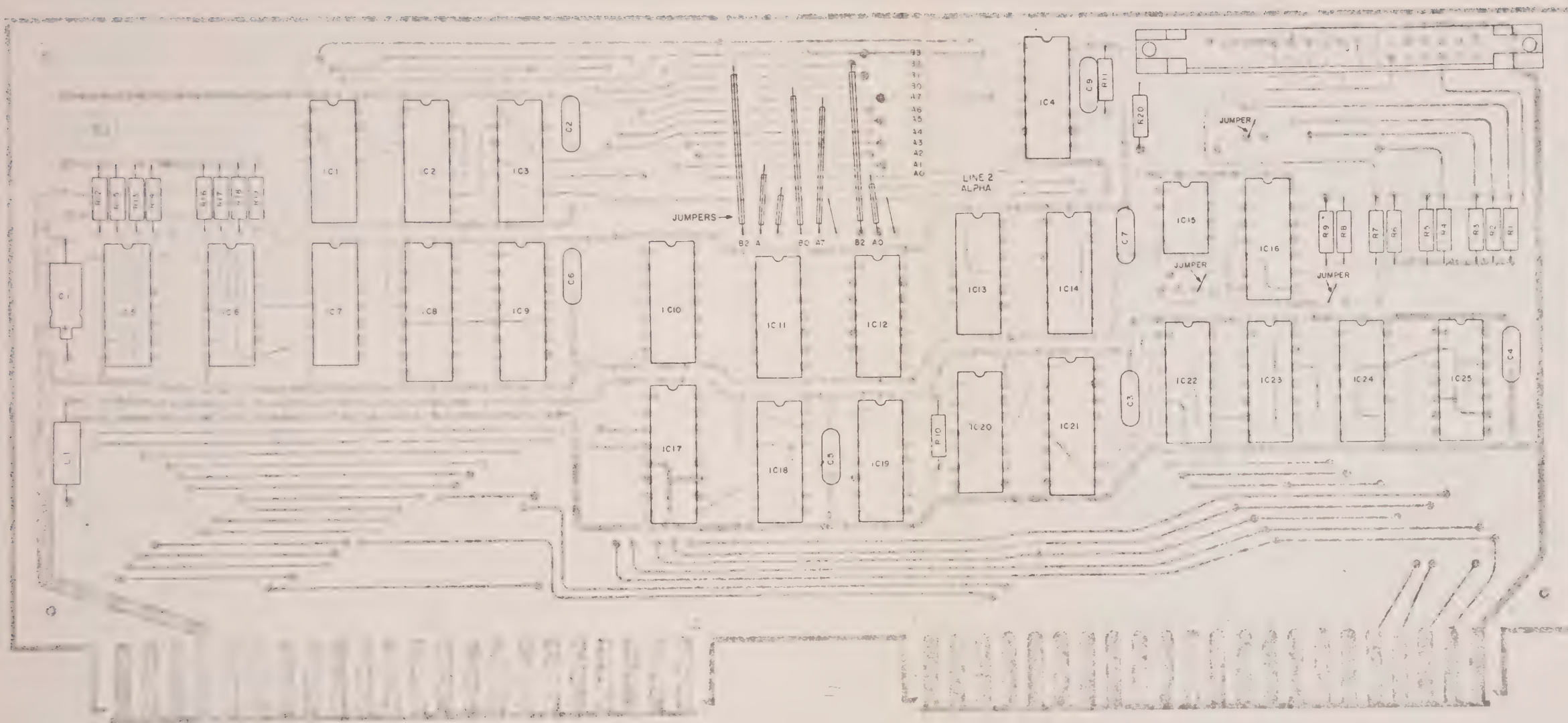
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00824	Resistor 820K $\frac{1}{4}$ W 5%	R10
611-00001	Resistor 4K .05%	R1
611-00002	Resistor 8K .1%	R2
611-00003	Resistor 16K .1%	R3
611-00004	Resistor 32K .1%	R4
616-00015	Resistor 165K 1/8W 1% MF	R7
616-00016	Resistor 316K 1/8W 1% MF	R8
616-00017	Resistor 3.32K 1/8W 1% MF	R25
616-00325	Resistor 4.22K 1/8W 1% MF	R31
616-00330	Resistor 6.19K 1/8W 1% MF	R26
616-00332	Resistor 9.09K 1/8W 1% MF	R29
616-00342	Resistor 40.2K 1/8W 1% MF	R5
616-00347	Resistor 80.6K 1/8W 1% MF	R6
663-00070	Transistor 2N3904	Q1-12
665-00078	IC MC3004P	IC 5
665-00079	IC N5741CT	IC 8
665-00110	IC MC 3002P	IC 12

ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
665-00112	IC MC 3008P	IC 13
665-00144	IC MC 4015P	IC9-11,14
665-00151	IC MC 4002P	IC 4
665-00145	IC MC 8309P	IC 6,7
665-00152	IC N8266B or MC7266P	IC 15
665-00153	IC N74157B or MC74157P	IC 1-3
495-00027	Amp Pins	XIC8
496-00043	Transistor Pad	XIC8

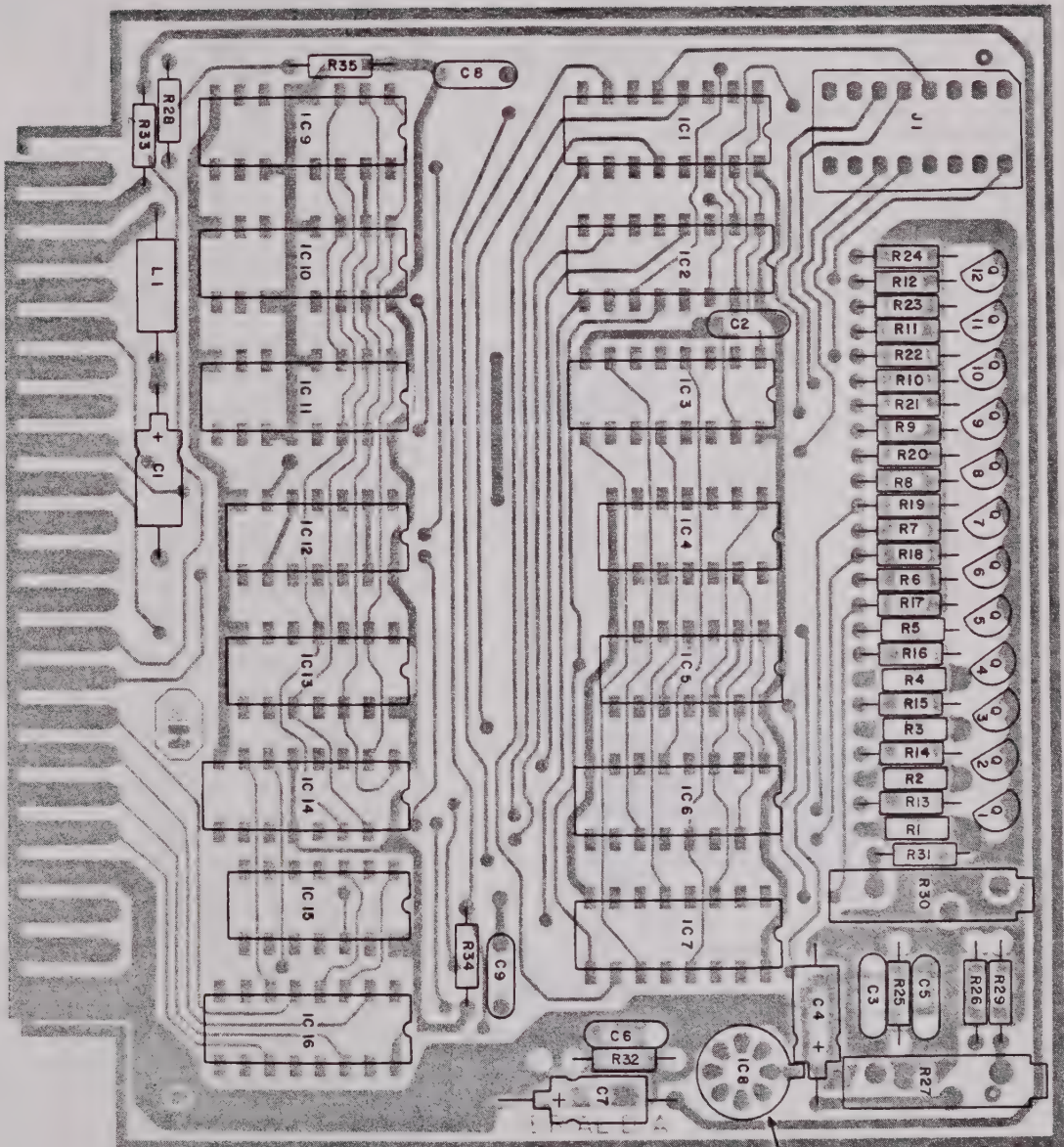






ASSEMBLY DRAWING
INTERFACE B (ASCII)

1501A
D 401-
22317 B

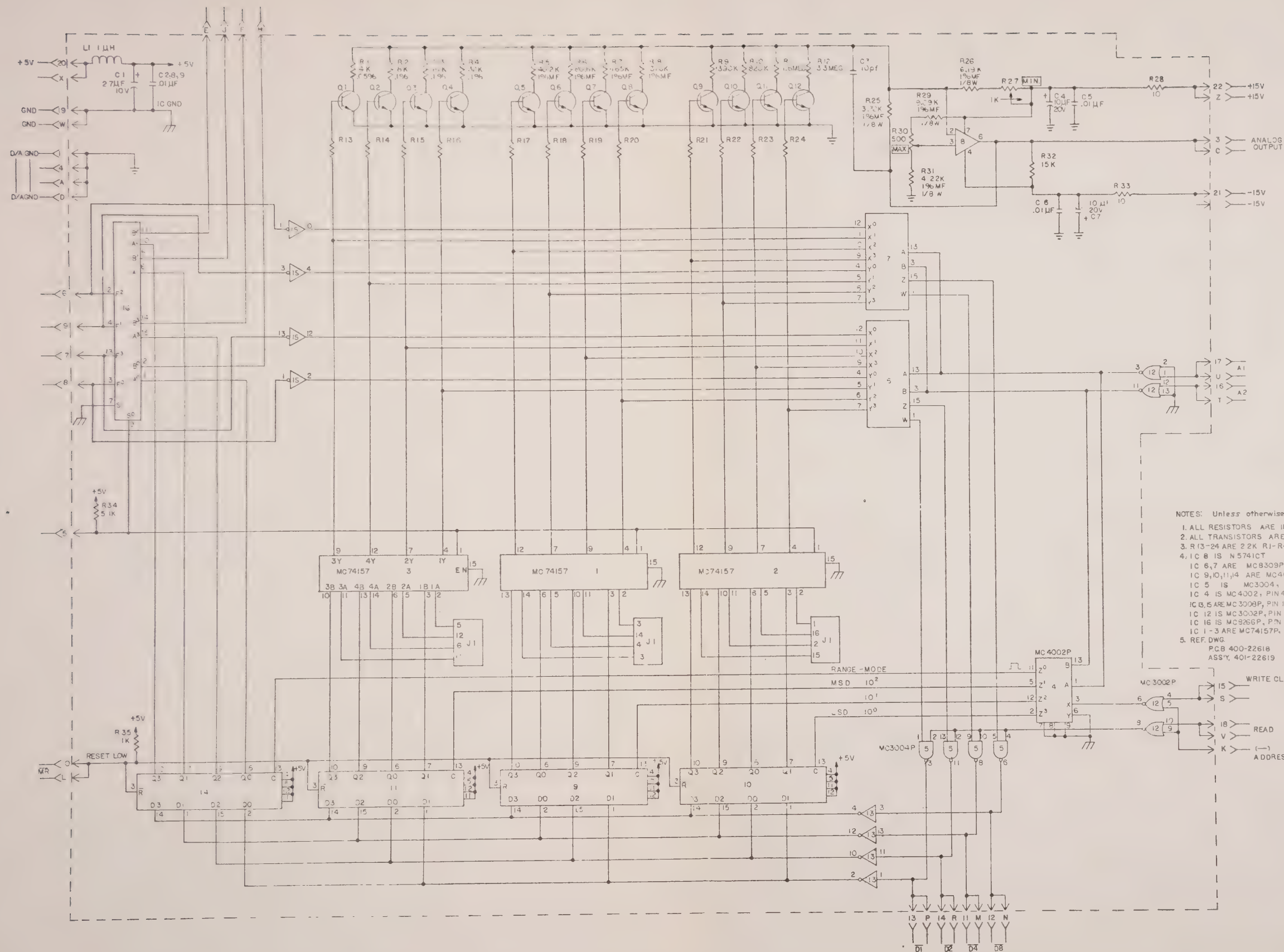


8 AMP PINS (495-00027 8)
1 TRANSISTOR PAD (496-00043)
UNDER THIS IC.

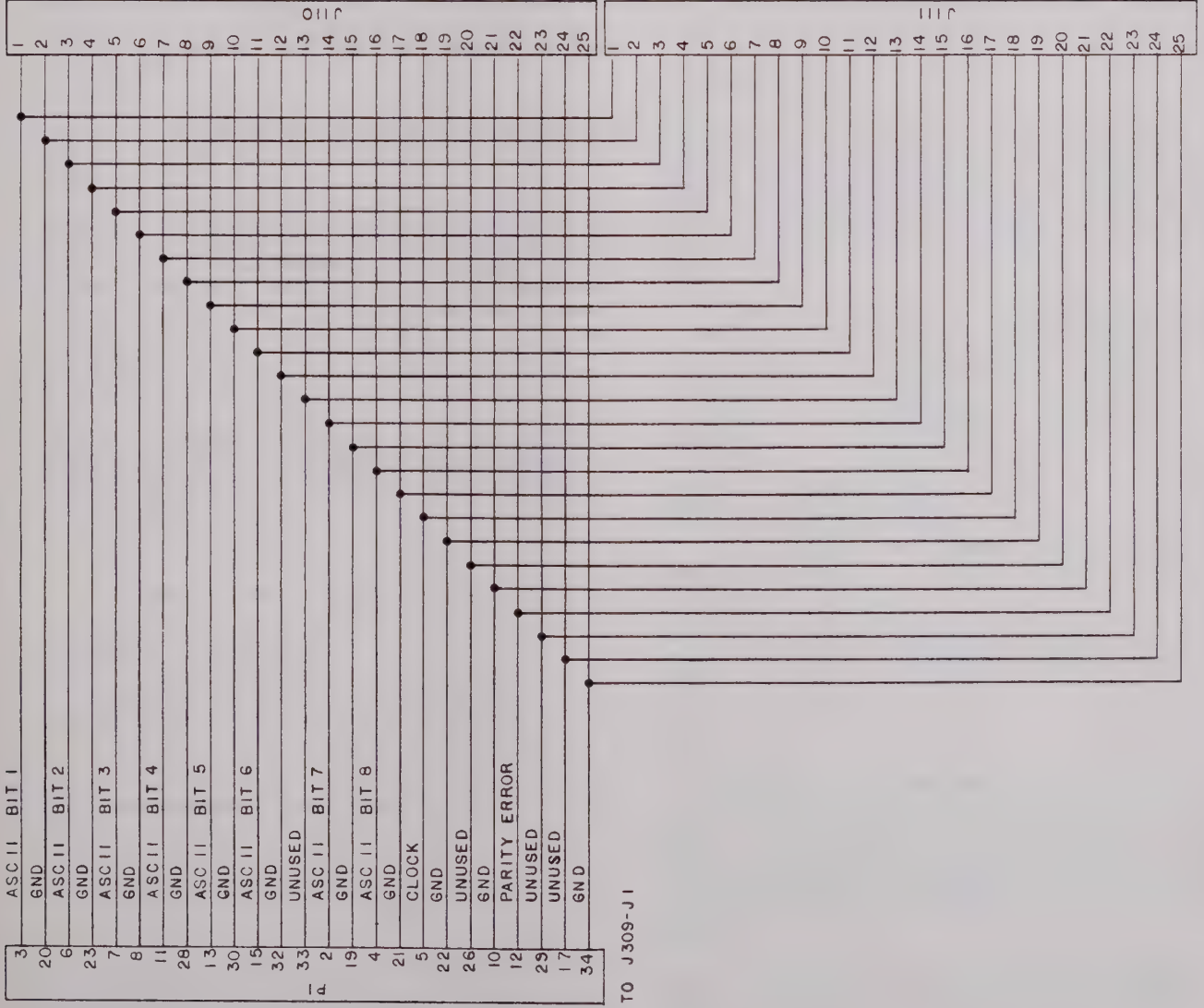
SERIAL D/A CONVERTER

MODEL NO. 1501A

C-401-22619 C



- NOTES: Unless otherwise noted
1. ALL RESISTORS ARE IN Ω , 1/4W, 5%
 2. ALL TRANSISTORS ARE 2N3904
 3. R13-24 ARE 2.2K R1-R4 ARE VISHAY V53-1
 4. IC 8 IS N5741CT
 5. REF. DWG.
- PCB 400-22618
ASSY. 401-22619



SCHEMATIC ASC II
SUB-PANEL REAR
1501 A
140-
C-22748 A

APPENDIX B

OPTION 01 SON

SERIAL BY 16-BIT WORD PROGRAMMING

B-1 GENERAL

The 16-bit serial by word option is designed for systems which incorporate a party-line data bus system where address and data are on separate lines. Data which was previously written in may be read out. This option also provides signals that can be used in request-answer closed loop systems.

Signals are TTL-compatible and ground true or positive true logic is selectable by internal wire straps. Data can be written in as fast as 1 μ s per word, or read out at 2 μ s per word. Miniature 50-pin feedthrough connectors are provided for easy party line connection. Data output is from open collector, NPN ground-emitter transistors, connected to the data input lines.

A data input word must always be 16 bits, one word per function. The data word contains one bit for mode control, three bits for range selection, and 12 bits for three digits of vernier control.

The address may be any number of bits from three to 16. In all cases, three adjacent bits are coded one through seven to select the seven pulse functions of the Model 1501A. Although these bits are defined as the three least significant bits, the user may connect them to any three bits as long as the code in Table B-1 is followed. The other 13 bits are independently definable. If only three bits of address are used, then a given 1501A must be controlled by either the Strobe pulse or the Write and Read lines.

The function address code and the 16-bit data word are defined in Table B-1. Table B-2 gives the range values and the decimal range number. As an example, for a frequency of 260 kHz, Internal Clock,

$$\text{frequency vernier} = 2 \times 260 = 520$$

	2^2	2^1	2^0	
ADDRESS -	X	X	X	0 0 1

	2^{15}		2^{11}		2^7		2^3	2^0							
DATA -	0	/	1	0	/	1	0	/	0	1	0	/	0	0	0

mode /	range /	-----	vernier	-----	/				
		5	/	5	/	.2	/	0	/

When writing in data, the address, data, and write line must be valid for 100 ns, minimum, before the Strobe, and must remain valid for 0.9 μ s after the Strobe.

When reading out data, the address and read lines must be valid for 100 ns minimum before the Strobe and remain valid for 0.9 μ s after the Strobe. The internal data will become valid on the data lines 0.8 μ s after the Strobe and remain valid for 1 μ s. The length of time the data is valid may be changed by adjusting the time constant R17-C1 shown on schematic diagram 140-22172. The time constant R15-C2 must also be changed if the FIN signal is used and it is desired to have the FIN signal occur near the end of the time that the data is valid.

If the Write or Read line goes false too soon, only partial data will be written in, and no data will be read out.

B-2 RESET MODES

When primary power is turned on, all internal storage is reset to zero, and the Model 1501A is in the following modes: maximum attenuation, inverted pulse mode, negative pulse, zero offset, Gate Off mode, frequency, delay, width, rise and fall times at minimum, internal clock, and single pulse. After initial programming, reset of internal storage can be done in two ways:

1) When eight lines are used for the address, a binary 255 address, a Write command, and a Strobe resets all registers to zero. This may be inhibited with an internal strap to ground; S4, shown on schematic diagram 140-22175.

2) One of the following, selected by wire straps on Address Board; S5, schematic diagram 140-22175.

a) Instrument address with the three least significant bits zero, and a Strobe.

b) Single external Master Reset line pulled to ground. The logic levels for the Master Reset are TTL-compatible (0 to +5 V).

Master Reset, BIZ, and FIN signals are always ground true. The Strobe, Read, Write, Address, and Data inputs can be selected for positive true or ground true.

B-3 ADDRESS (Refer to schematic diagram 140-22175)

Each bit is selected individually by switches S1 and S2 mounted on the Address Board. For ground true logic, switches S1-a, S1-b, and S1-c must be closed to ground. The other switches will be closed or open if a bit is "1" or "0" respectively. For positive true logic, the switch positions are reversed.

If reset on address 255 is used, switch S3 is strapped to ground for ground true logic, or left open for positive true logic. If it is desired to inhibit reset on address 255, switch S4 is strapped to ground.

B-4 DATA LOGIC POLARITY(Refer to schematic diagram 140-22172)

All data bits for input data are selected by grounding S1 for ground true data or leaving S1 open for positive true data.

Ground true output data is selected by leaving S2 open. For positive true output data, S2 is strapped to ground. It should be noted that output data is from open collector NPN transistors and is valid only during the time indicated in the timing diagram. It should also be noted that there are no pull-up resistors in the data input/output lines.

B-5 STROBE, READ, WRITE LOGIC POLARITY(Refer to schematic diagram 140-22172)

These three signals must have the logic true levels, and are set by switch S3. If S3 is set to ground, the levels are ground true, and if left open, the levels are positive true.

B-6 SIGNAL INPUT LOADING

A low level (ground) is equal to or less than 0.5V. A high level is +2.5 V minimum to +5 V maximum. A low level must not go more than 0.5 V below ground.

Address and data bits have a maximum loading in the high state of 250 μ A.

Strobe, Read, and Write are each one TTL load plus a 5.1K resistor to +5 V.

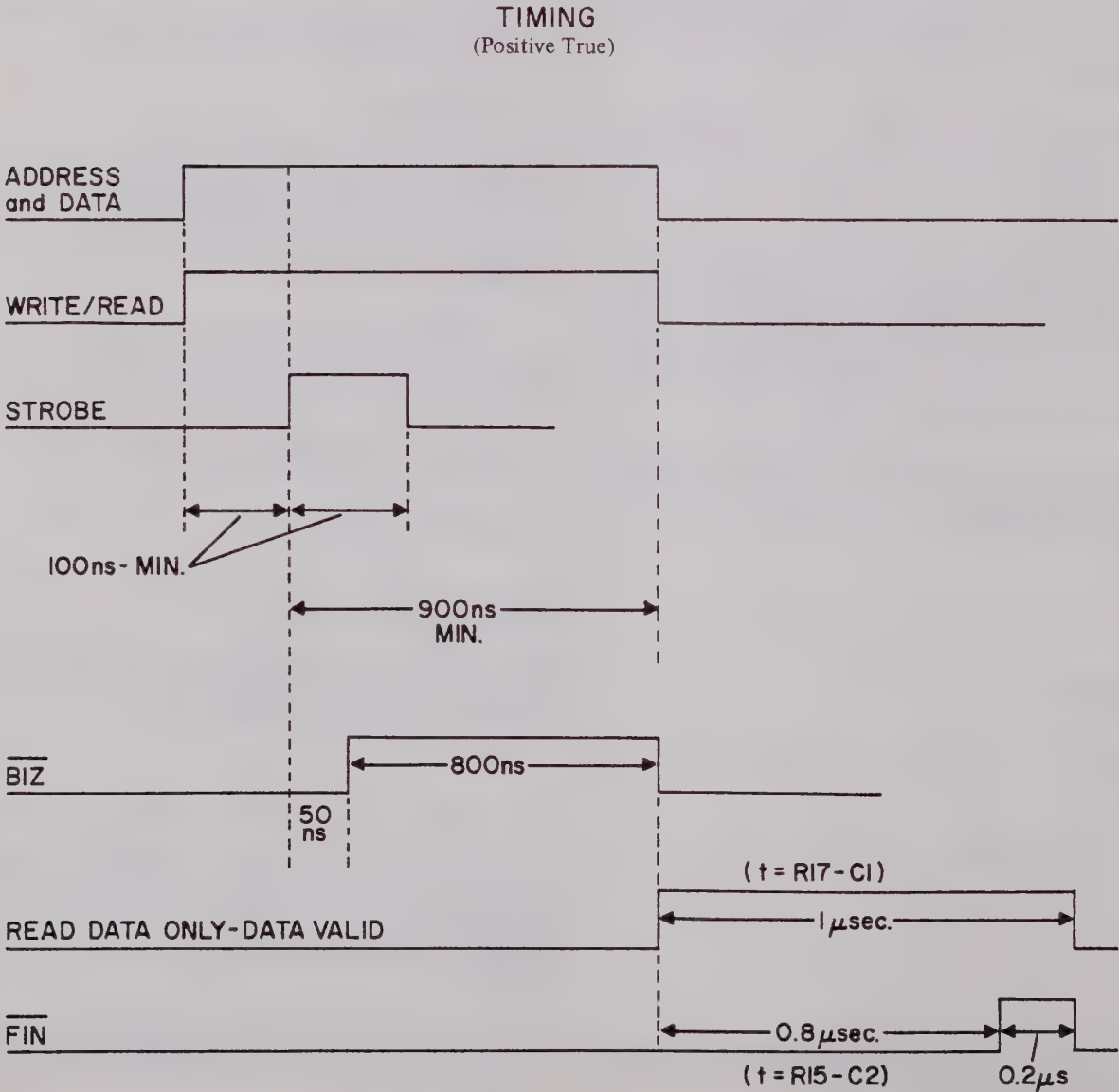
Strobe, Read, and Write are each one TTL load plus a 5.1K resistor to +5 V.

When the master reset line is used, it is two TTL loads plus a 1K resistor to +5 V.

B-7 SIGNAL INPUT CONNECTIONS

Address and Data connections are listed in Table B-3.

Figure B-1. Timing Diagram



B-8 1501A - SERIAL BY WORD INTERFACE CIRCUIT DESCRIPTION

a. Address Card J309A (Refer to Schematic 140-22175)

(1) **General.** The address lines are buffered by IC's 3, 6, 8, and 10. These are 2 input positive AND gates. They present a maximum D.C. load of 250 μ A when their input is in the high state.

The outputs from these IC's go to exclusive NOR gates for true logic level selection. These gates are IC's 2, 5, 7, and 9. Their output is always high state true.

The three least significant bits are decoded by IC 13, a 1-of-8 decoder. The output from IC 13 is ground true and is enabled via pin 7 when the rest of the address bits are true. The exclusive NOR gates are open-collector so that any one being in the low state holds pin 7 of IC 13 low, which inhibits any of the address lines from going low.

When a proper address is decoded, pin 7 of IC 13 is pulled high and also pin 9 of IC 12. IC 12-pin 8 then goes low which allows a strobe pulse to start a read or write sequence.

(2) **Reset Modes.** IC 1 and IC4 are connected to decode the binary address 255. The three least significant bits are gated with the write signal so that, with a strobe pulse to pin 2 of IC 11, a reset signal is generated. S-3 is strapped to ground if the address input is ground-true logic. S-4 is strapped to ground if address 255 is not used as a system reset.

The three least significant bits, decoded by IC-13 can also be used as a reset signal by connecting pin 3 of IC 13 to pin 2 of IC-12. This causes pin 3 of IC-12 to go positive so that a strobe pulse on pin 2 of IC-11 will generate a reset pulse.

An external Master Reset line is provided on pin 1 of the connector. This line is activated in the low state. To use this reset mode, connect S-5 between pin 1 of IC-11 and pin 2 of IC-12. This will then produce a reset pulse from IC-11 independent of any other input signals.

The power-on reset is generated by C1 holding down pin 4 of IC-12. Pin 6 is forced to a high state which turns on Q1 long enough for all power supplies to attain their steady-state operating values.

The width of the reset pulse is determined by C3 and R24. This width should be greater than 80 ns. With the component values shown, the width at pin 6 of IC-11 will be 100 ns $\pm$ 20 ns. The width at pin T of the circuit board will in general be much wider, due to the storage time of Q1.

b. **Data Card**-(Refer to Schematic 140-22172). The data logic provides the control for the flow of data to the storage registers in groups of four bits when writing into the instrument, and constructing a 16-bit parallel word when reading the data stored in the instrument.

The read, write, and strobe signals go through exclusive NOR gates in IC 25 for logic true level selection.

In order to do a write sequence, the address and data lines, and the write signal should be allowed to settle for a minimum of 100 ns, before a strobe is sent to the interface. The write signal, being high at the output of IC 25, pin 3,

causes pin 5 of IC-1 to be low and therefore inhibit the read sequence. The read line should be low so pin 9 of IC 1 is high. With a valid address being low, a strobe pulse is differentiated through IC-13, pin 1, and IC-2, pins 12 and 13. (See Figure B-2, part 1.) The output from IC-2, pin 11, will be a negative-going spike, which forces pin 6, IC-2 high. IC-1 pin 12 goes high, and because all the inputs to that gate are high at this time, the output, pin 8, IC-1 goes low. This initiates the write sequence.

At the time of the negative spike on IC-2 pin 11, pin 10 of IC-2 is high so pin 8 of IC-2 will go negative thus holding pin 6, IC-2 positive.

When IC-1, pin 8 goes negative, IC-4, pin 6 goes positive, removing the reset on the binaries IC-28, and IC-16, and allowing the multivibrator, IC 3, to start running, via pin 3, IC-3. IC-1, pin 8, also allows write clocks to pass through IC-13 pin 10, and gates the input data through IC-18.

The two binaries of IC-28 select four bits at a time via the data selectors IC 6 and IC 7. They also select the proper four bits of storage on the D/A cards via the address lines from IC-26, pins 8 and 11.

The write sequence is terminated when pins 5 and 9 of IC-28 are both high, presenting a high input to binary IC-16. This high input cause this binary to be set. Pin 5 of IC-16 goes high, forcing pin 11 of IC 13 low which then resets the input flip-flop, pins 6 and 8 of IC-2. IC-4, pin 6 goes low, turning off the multivibrator, IC-3, and resets the binaries, IC 16 and IC 28.

The write clocks at pin A-S, are negative going. (See Figure B-2, part 2.) The first character, 4 bits, of data, is strobed into the registers on the negative going edge. When this clock waveform goes positive, the address binaries of IC-28, change state. The next character is then gated onto the common data lines $\overline{D1}$, $\overline{D2}$, $\overline{D4}$, and $\overline{D8}$.

(1) **Multivibrator Timing.** The quiescent state of the multivibrator, IC-3, is with pin 8 low, and pin 6 high. Pin 4 will also be high, being connected to pin 6 via R10. When pin 3 goes high, pin 8 goes high, and the timing state (determined by C6 and R19 and R20) is started. Pin 6 goes low and discharges C5 through the diode. At the end of the timing state, pin 6 goes high and pin 4 goes high after a time determined by C5 and R10, and the input threshold of the IC. This delays the start of the next timing state to allow settling time of the address and data.

R20 should be adjusted by observing the wave form either at pin 3 of IC-14, or pin A-S. Adjust R20 so that the time between the first negative-going edge and the fourth negative-going edge is 0.6 μ sec. The time that the wave form is at the high level is determined by C5 and R10, and should be 80 ns to 100 ns.

During a normal cycle, the clock waveform should return to the high level approximately 100 ns after the fourth negative transition. See Figure B-2, part 2.

(2) **Read Sequence.** With the read line in the true state, pin 4 of IC 1 will be high so that when pin 6 of IC-2 goes high with a strobe, pin 6 of IC-1 will go low, initiating a Read cycle.

As in a write cycle, the multivibrator is started and binaries, IC-28 address the characters. With the address lines on A-A and A-B, the function address line from the address card, and

the read signal on pin A-P, the characters are strobed 4 bits at a time, into the D-flip-flops in IC's 19, 20, 31, and 32. The strobes to the D flip-flops are routed by IC-29 and address binaries, IC-28. The first strobe goes to IC-32, the second to IC-31, third to IC-20, and the fourth to IC-19. The characters are thus set up in the same order as when they are written in, most significant bits first, i.e., Mode bit and Range bits first.

The data at the inputs to gates IC-30 is ground true. For ground true data out, S-2 must be open so that pins 1, 5, 13, and 10 are high.

When the read sequence ends, IC-16, pin 6 goes momentarily low which triggers the two one-shots, IC-15. The output, pin 13, of IC-15 goes high forcing pin 8 of IC 4 low, which gates the 16 bits of data onto the data buss via IC's 34 thru 40. These are open collector power gates, which are in the low state with both inputs low.

Note that during a write cycle, pin 8 of IC4 will not go low because pin 6 of IC-5 will not be high. Pin 6 is high during a read cycle via pin 6 of IC-1, and pins 8 and 11 of IC-5. C4

and R13 ensure that pin 4 of IC-5 is low when pin 13 of IC-4 goes high at the end of the Read cycle.

The readout data is valid for the timing state at pin 13 of IC-15. This is normally set for 1 use, but may be set for any time required.

The FIN signal is low state true, and begins at the trailing edge of pin 12, IC-15, and ends at the trailing edge of pin 4, IC-15.

As indicated above, the strobes to the D-flip-flops of IC's, 19, 20, 31, and 32 are distributed through IC-29. The proper waveforms during a Read cycle are shown on Figure B-2, part 3.

If the write or read line goes false before the end of a cycle, pin 6, IC-4, will go negative and be differentiated through pin 5, IC-13, and pins 9 and 10, IC-12. This causes pin 11 of IC-13 to go negative which then ends the cycle. If this occurs, only partial data is written in, and no data will be gated out.

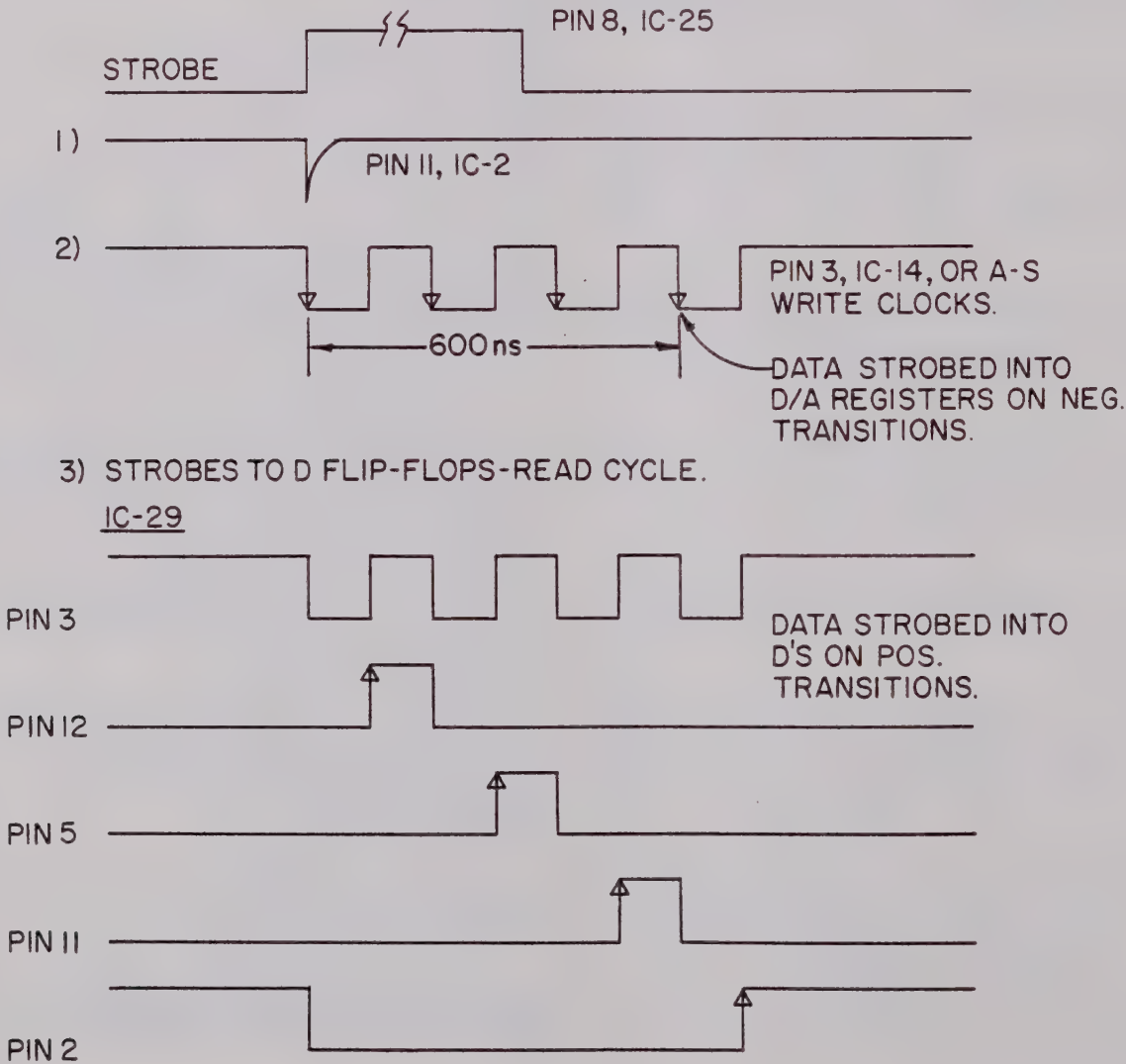


Figure B-2 Waveforms - Schematic 140-22172

Table B-1. Function Address and Data Input

Function	Address	16-Bit Data Word			
	X X 3 dependent bits	Mode bit	Range Char.	3 BCD Digits Vernier	
	2 ² 2 ¹ 2 ⁰	2 ¹⁵	2 ¹⁵ 2 ¹⁴ 2 ¹³ 2 ¹²	2 ¹¹ ---- 2 ⁰	
Frequency	X X 0 0 1	0/1 int/ext	Table B-2		
Delay	X X 0 1 0	sgl/dbl	Table B-2		
Width	X X 0 1 1	inv/norm	Table B-2		
Ldg Edge	X X 1 0 0	norm/gate on	Table B-2		
Trlg Edge	X X 1 0 1	not used	not used		
Offset	X X 1 1 0	not used	0 1 0 = pos 1 0 0 = neg		
Amplitude	X X 1 1 1	neg/pos pulse pol	Attenuation Table B-2		

Table B-2 Range Programming

Function	Range Value	Range	Vernier
Frequency	0	0.5 Hz-4.995 Hz	100-999
	1	5 Hz-49.95 Hz	100-999
	2	50 Hz-499.5 Hz	100-999
	3	500 Hz-4.995 kHz	100-999
	4	5 kHz-49.95 kHz	100-999
	5	50 kHz-499.5 kHz	100-999
	6	500 kHz-4.995 MHz	100-999
	7	5 MHz-49.95 MHz	100-999
Delay/Width	0	10 ns-99.9 ns	100-999
	1	100 ns-999 ns	100-999
	2	1 μ s-9.99 μ s	100-999
	3	10 μ s-99.9 μ s	100-999
	4	100 μ s-999 μ s	100-999
	5	1 ms-9.99 ms	100-999
	6	10 ms-99.9 ms	100-999
	7	100 ms-999 ms	100-999
Ramp Rate	0	uncalibrated range*	100-999
	1	0.1-0.999 V/ns	100-999
	2	10.0-99.9 V/ μ s	100-999
	3	.0-9.99 V/ μ s	100-999
	4	0.1-0.999 V/ μ s	100-999
	5	10.0-99.9 V/ms	100-999
Attenuation	0	(x 128) 40-80 mV	000-999
	1	(x 64) 80-156 mV	000-999
	2	(x 32) 156-312 mV	000-999
	3	(x 16) 312-625 mV	000-999
	4	(x 8) 0.62-1.25 V	000-999
	5	(x 4) 1.25-25 V	000-999
	6	(x 2) 2.5-5.0 V	000-999
	7	(x 1) 5.0-10.0 V	000-999

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table B-3 Data and Address Input/Output

ADDRESS - J110 and J111

Pin	Signal	Pin	Signal
1	Master Reset	14	2 ¹²
2	2 ⁰	15	2 ¹³
3	2 ¹	16	2 ¹⁴
4	2 ²	17	2 ¹⁵
5	2 ³	18	not used
6	2 ⁴	19	Strobe
7	2 ⁵	20	BIZ
8	2 ⁶	21	FIN
9	2 ⁷	22	not used
10	2 ⁸	23	WRITE
11	2 ⁹	24	READ
12	2 ¹⁰	25	not used
13	2 ¹¹	26-50	ground

DATA - J112 and J113

Pin	Signal	Pin	Signal
1	not used	8	2 ⁶
2	2 ⁰	9	2 ⁷
3	2 ¹	10	2 ⁸
4	2 ²	11	2 ⁹
5	2 ³	12	2 ¹⁰
6	2 ⁴	13	2 ¹¹
7	2 ⁵	14	2 ¹²
15	2 ¹³	26-50	ground
16	2 ¹⁴		
17	2 ¹⁵		
18-25	not used		

Rear-Panel Input/Output Connections (All Type BNC)

Ext Drive In	J105
Trigger Out	J103
Async. Gate In	J106
Sync. Gate In	J107
Pulse Output	J108

NOTE

Analog Control connector J109 is not used in Model 1501A's with serial by 16-bit word programming.

ASSEMBLY NO. 350-21903DESCRIPTION MOD KIT/16 BIT DATA/8 BIT ADDRESS
GND TRUE BCD

ASSEMBLY NO. PART NO.	DESCRIPTION	SCHEMATIC REF.
	ADD	
400-22619	D/A Serial Board Assembly	J305-307 J311-314
400-22930	8 Bit Address Bd. Assembly	J309
249-21385	Sub Panel Rear Assembly	
400-22171	SI Interface Board Assy.	J308
	ADD TO 820-21290	
140-26043	Doc List	Prod Ref
700-00034	Connector, 50 Pin Amphenol	
	DELETE	
401-21212	D/A Parallel Board Assy	J305-307 311-314
249-21283	Sub Panel Rear Assembly	
	DELETE FROM 820-21290	
700-00024	Connector, 24 Pin Amphenol	

ASSEMBLY NO. 401-22930DESCRIPTION 8 BIT ADDRESS BOARD ASSEMBLY

ASSEMBLY OR PART NO	DESCRIPTION	SCHEMATIC REF.
400-221 3	PC Board	
401-22930	Assembly Drawing	Prod Ref
140-22931	Schematic	Prod Ref
311-00041	Cap, Cerm .1 μ f 12V	C4
311-00003	Cap, Cerm 25pf	C3
318-00005	Cap, Tant 10 μ f 20V	C2
318-00019	Cap, Tant 47 μ f 20V	C1
335-00022	Choke, 1 μ h	L1
376-00022	Diode, 1N914B	CR1
595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R19-23, 27-35
595-00103	Resistor 10K $\frac{1}{2}$ W 5%	R25,37
595-00331	Resistor 330 Ω $\frac{1}{2}$ W 5%	R17,26,36
595-00511	Resistor 510 Ω $\frac{1}{2}$ W 5%	R18
595-00512	Resistor 5.1K $\frac{1}{2}$ W 5%	R9-16,24
624-00060	AMP 435166-5 Switch, D.I.P., 8 Position	S1
624-00061	Cover D.I.P. Switch8 Position AMP 435238-5	XS2

ASSEMBLY NO. 401-22930DESCRIPTION 8 BIT ADDRESS BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
663-00124	Transistor 2N4401	Q1
665-00053	IC MC 3000P	IC 12
665-00123	IC MC 4038P	IC 13
665-00130	IC MC 8601P	IC11
665-00134	IC SP384A	IC3,6
665-00154	IC MC 7242P	IC1,2,4,5
700-00144	Header, 50 Pin 3M-3433-2002	J1

ASSEMBLY NO. 249-21385DESCRIPTION ASSEMBLY SUB-PANEL REAR

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
248-2138	Panel	
144-21383	Silkscreen, Panel	Prod Ref
706-21379	Cable Assy, Dual 50 Pin	J112,J113
706-21380	Cable Assy, Dual 50 Pin	J110,J111
201-00004	Screw, 3-48x $\frac{1}{2}$ BHMS (8)	Prod Ref
215-00002	Lockwasher #3 (8)	Prod Ref
240-00019	Hex Nut #3-48 (8)	Prod Ref

ASSEMBLY NO. 401-22171DESCRIPTION S-1 INTERFACE BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22170	PC Board	
401-22171	Assembly Drawing	Prod Ref
140-22172	Schematic	Prod Ref
311-00003	Cap, Cerm 25pf 1KV 10%	C6
311-00006	Cap, Cerm 50pf 1KV 10%	C1,2
311-00007	Cap, Cerm 100pf 1KV 10%	C4,7,13
311-00009	Cap, Cerm 500pf 1KV 10%	C3,5
311-00074	Cap, Cerm, .01 μ f 100V	C9-12
318-00005	Cap, Tant 10 μ f 20V	C8
335-00022	Choke, 1 μ h	L1
376-00022	Diode, 1N914B	CR1
551-00041	Potentiometer 5K 89PR	R20
551-00055	Potentiometer 50K 89PR	R15,17
595-00101	Resistor 100 Ω $\frac{1}{2}$ W 5%	R13,14,21
595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R1-6,9
595-00221	Resistor 220 Ω $\frac{1}{2}$ W 5%	R10
595-00472	Resistor 4.7K $\frac{1}{2}$ W 5%	R16,18
595-00512	Resistor 5.1K $\frac{1}{2}$ W 5%	R19,22-25

ASSEMBLY NO. 401-22171DESCRIPTION S-1 INTERFACE BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
665-000 3	IC MC 3000P	IC2,5,12, 14,26
665-00054	IC MC 3061P	IC 16,28
665-00078	IC MC 3004P	IC 18
665-00084	IC MC 3022P	IC8,9,21, 22,25,30
665-00100	IC SN75453P	IC33-40
665-00110	IC MC 3002P	IC 13,17
665-00144	IC MC 4015P	IC19,20, 31,32
665-00130	IC MC8601P	IC 3
665-00133	IC SN75452P	IC 27
665-00134	IC SP384A	IC10,11, 23,24
665-00139	IC SN74123N	IC 15
665-00146	IC MC 3024P	IC 1,4
665-00151	IC MC 4002 P	IC 29
665-00145	IC MC8309P	IC 6,7
700-00144	Header, 3M 50 Pin 3433-2002	P1

ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

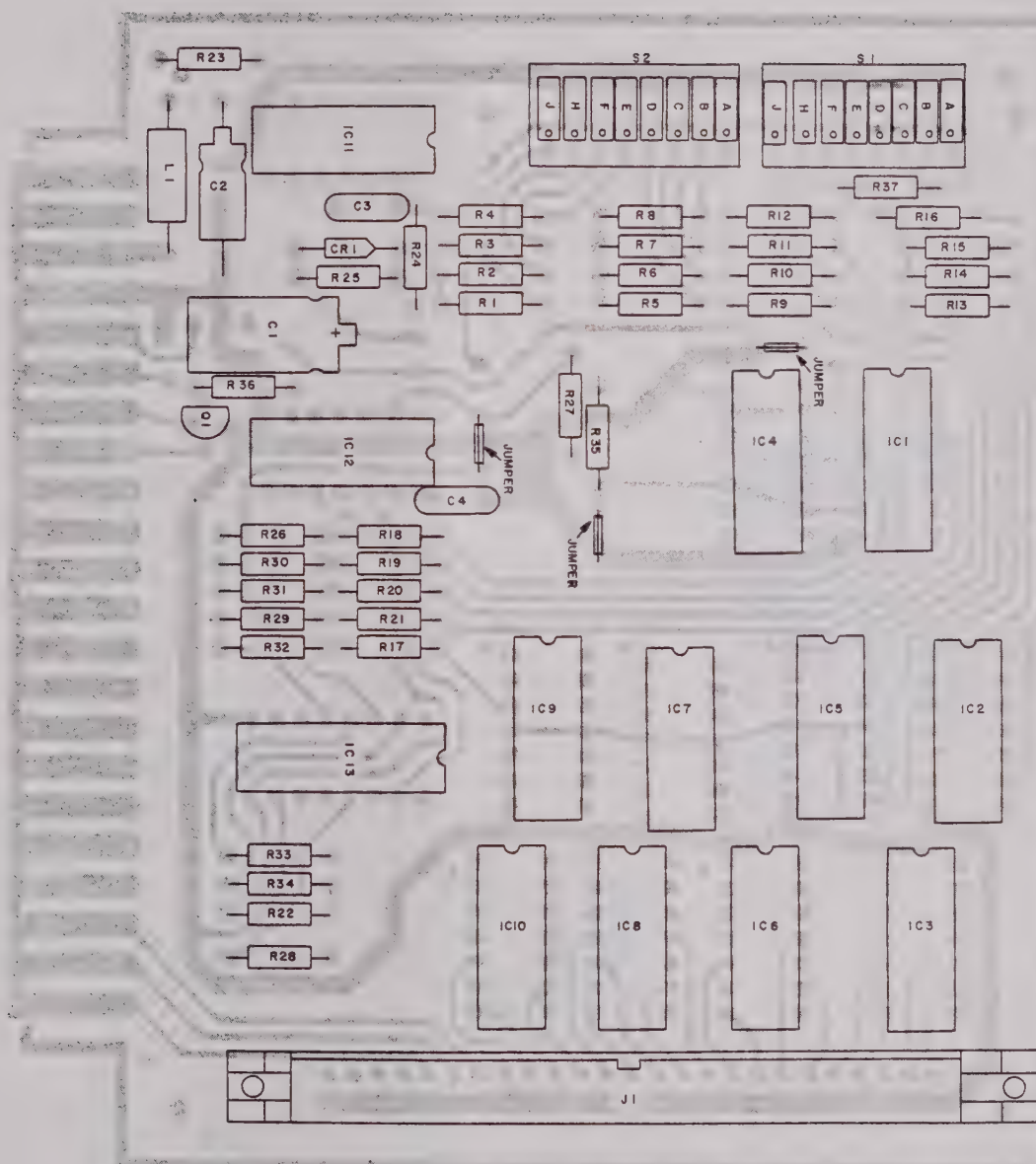
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22618	PC Board	
401-22619	Assembly Drawing	Prod Ref
140-22620	Schematic	Prod Ref
311-00001	Cap, Cerm 10pf 1KV	C3
311-00074	Cap, Cerm .01 μ f 100V	C2,5,6, 8,9
318-00004	Cap, Tant 27 μ f 10V	C1
318-00005	Cap, Tant 10 μ f 20V	C4,7
335-00022	Choke 1.0 μ h	L1
495-00054	Socket, IC 16 Pin	J1
595-00102	Resistor 1K $\frac{1}{4}$ W 5%	R35
551-00035	Potentiometer 00 Ω 89PR	R30
551-00040	Potentiometer 1K 89PR	R27
595-00100	Resistor 10 Ω $\frac{1}{4}$ W 5%	R28,33
595-00153	Resistor 15K $\frac{1}{4}$ W 5%	R32
595-00165	Resistor 1.6M $\frac{1}{4}$ W 5%	R11
595-00222	Resistor 2.2K $\frac{1}{4}$ W 5%	R13-24
595-00335	Resistor 3.3M $\frac{1}{4}$ W 5%	R12
595-00394	Resistor 390K $\frac{1}{4}$ W 5%	R9
595-00512	Resistor 5.1K $\frac{1}{4}$ W 5%	R34

ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

ASSEMBLY OP PART NO	DESCRIPTION	SCHEMATIC REF.
595-008.4	Resistor 820K $\frac{1}{2}$ W 5%	R10
611-00001	Resistor 4K .05%	R1
611-00002	Resistor 8K .1%	R2
611-00003	Resistor 16K .1%	R3
611-00004	Resistor 32K .1%	R4
616-00015	Resistor 165K 1/8W 1% MF	R7
616-00016	Resistor 316K 1/8W 1% MF	R8
616-00017	Resistor 3.32K 1/8W 1% MF	R25
616-00325	Resistor 4.22K 1/8W 1% MF	R31
616-00330	Resistor 6.19K 1/8W 1% MF	R26
616-00332	Resistor 9.09K 1/8W 1% MF	R29
616-00342	Resistor 40.2K 1/8W 1% MF	R5
616-00347	Resistor 80.6K 1/8W 1% MF	R6
663-00070	Transistor 2N3904	Q1-12
665-00078	IC MC3004P	IC 5
665-00079	IC N5741CT	IC 8
665-00110	IC MC 3002P	IC 12

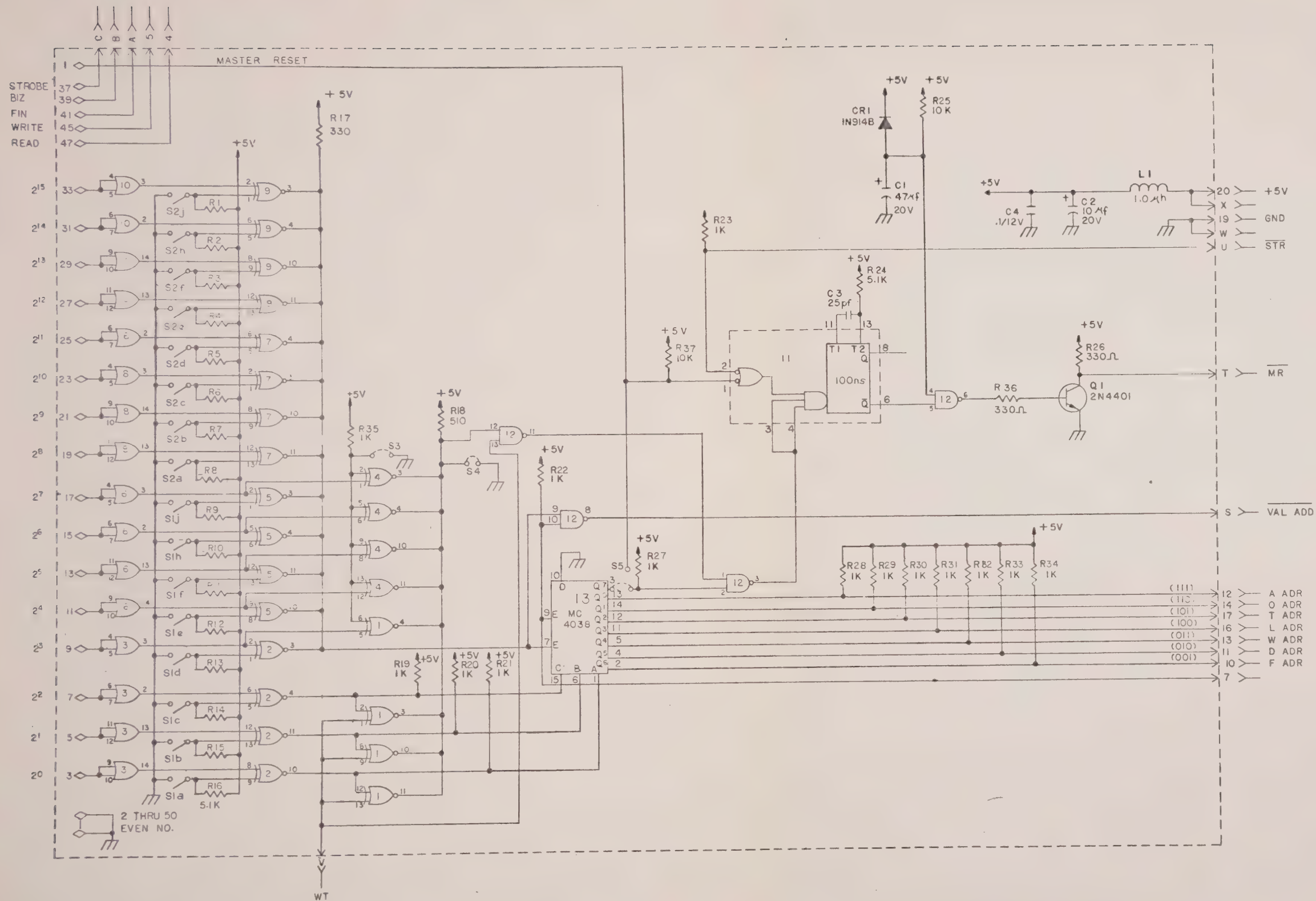
ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER RCD ASSEMBLY

ASSEMBLY OR P/	DESCRIPTION	SCHEMATIC REF.
565-00112	IC MC 3008P	IC 13
565-00144	IC MC 4015P	IC9-11,14
565-00151	IC MC 4002P	IC 4
565-00145	IC MC 8309P	IC 6,7
565-00152	IC N8266B or MC7266P	IC 15
565-00153	IC N74157B or MC74157P	IC 1-3
95-00027	Amp Pins	XIC8
496-00043	Transistor Pad	XIC8



ASSEMBLY DRAWING
16 BIT ADDRESS BOARD

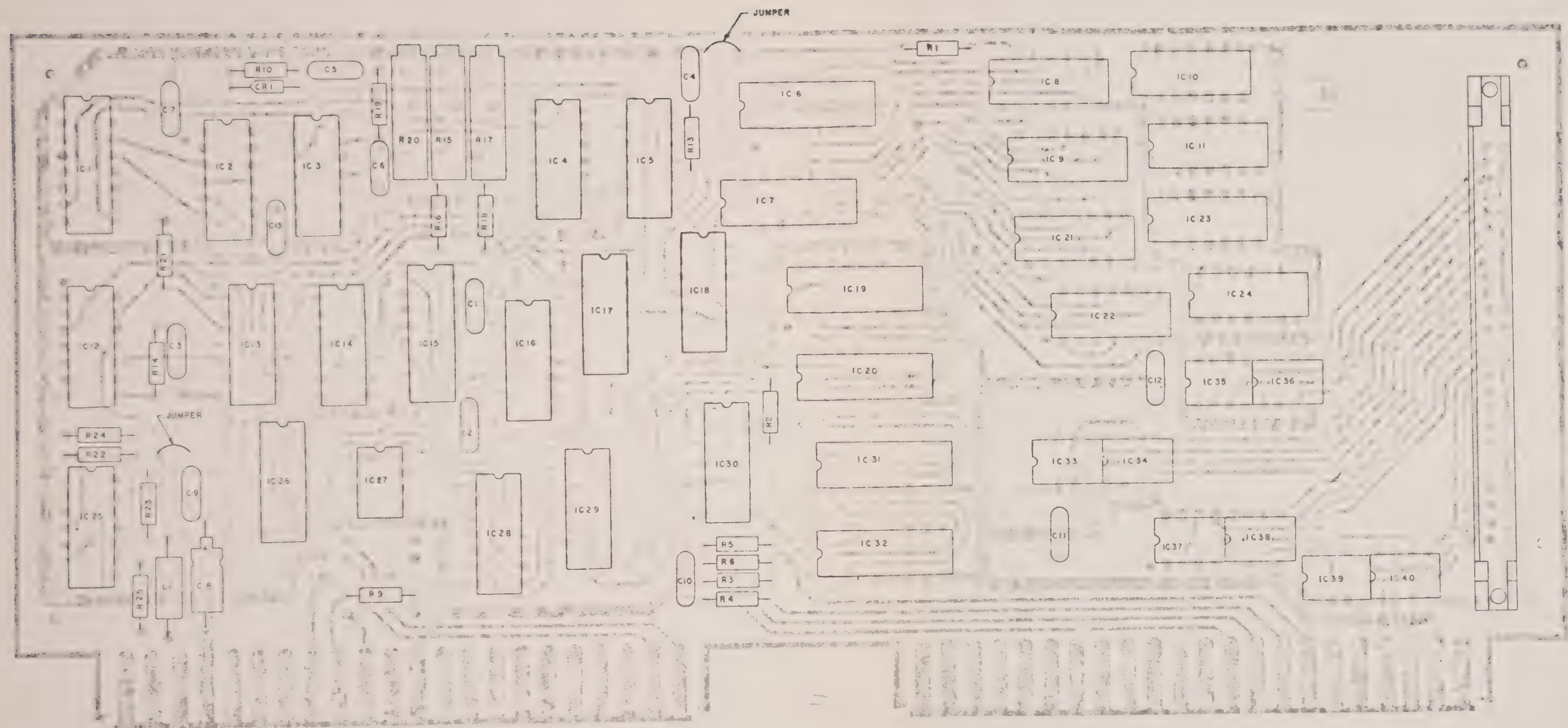
MODEL 1501A
C-401-
22174 A

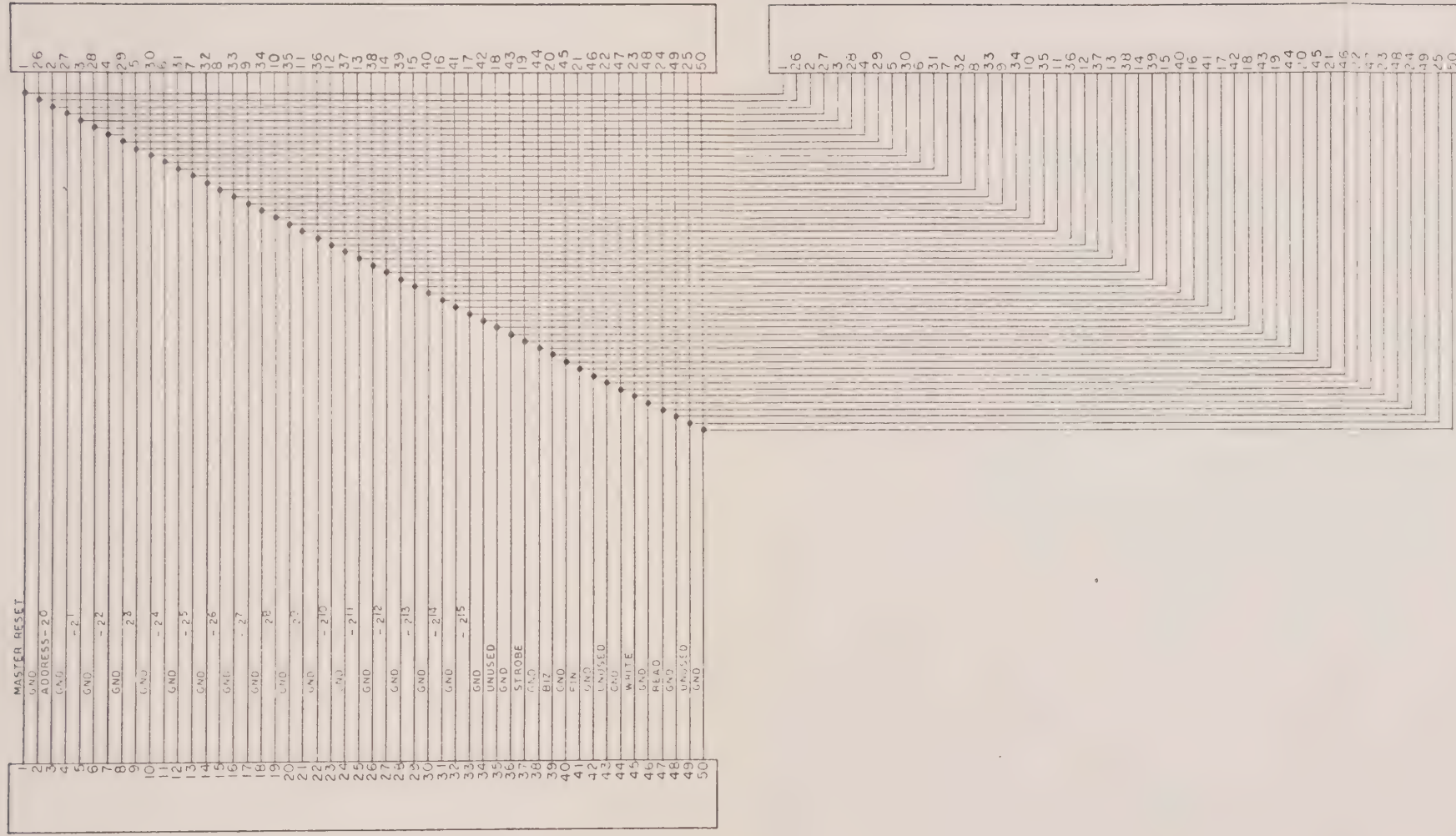


- NOTES:
1. IC 1,2,4,5,7,9 ARE MC7242P PIN 7 TO GND PIN 14 TO Vcc.
 2. IC 3,6,8,10, ARE SP384 PIN 1 TO GND PIN 8 TO Vcc.
 3. IC 11 IS MC8601P PIN 7 TO GND PIN 14 TO Vcc.
 4. IC 12 IS MC3000P PIN 7 TO GND PIN 14 TO Vcc.
 5. IC 13 IS MC4038P PIN 8 TO GND PIN 16 TO Vcc.
 6. S3 TO GND. FOR NEG.TRUE LOGIC.
 7. S4 TO GND. TO INHIBIT 255 RESET.
 8. S5 TO R27 FOR MASTER RESET.
 9. S5 TO PIN 3, IC13, FOR RESET ON (000)-3LSB'S- OF ADDRESS.
 10. REF.DWGS.
- FAB. 400-22173
ASS'Y. 140-22174

SCHEMATIC
16 BIT
ADDRESS BOARD

1501A
140-
22175 A



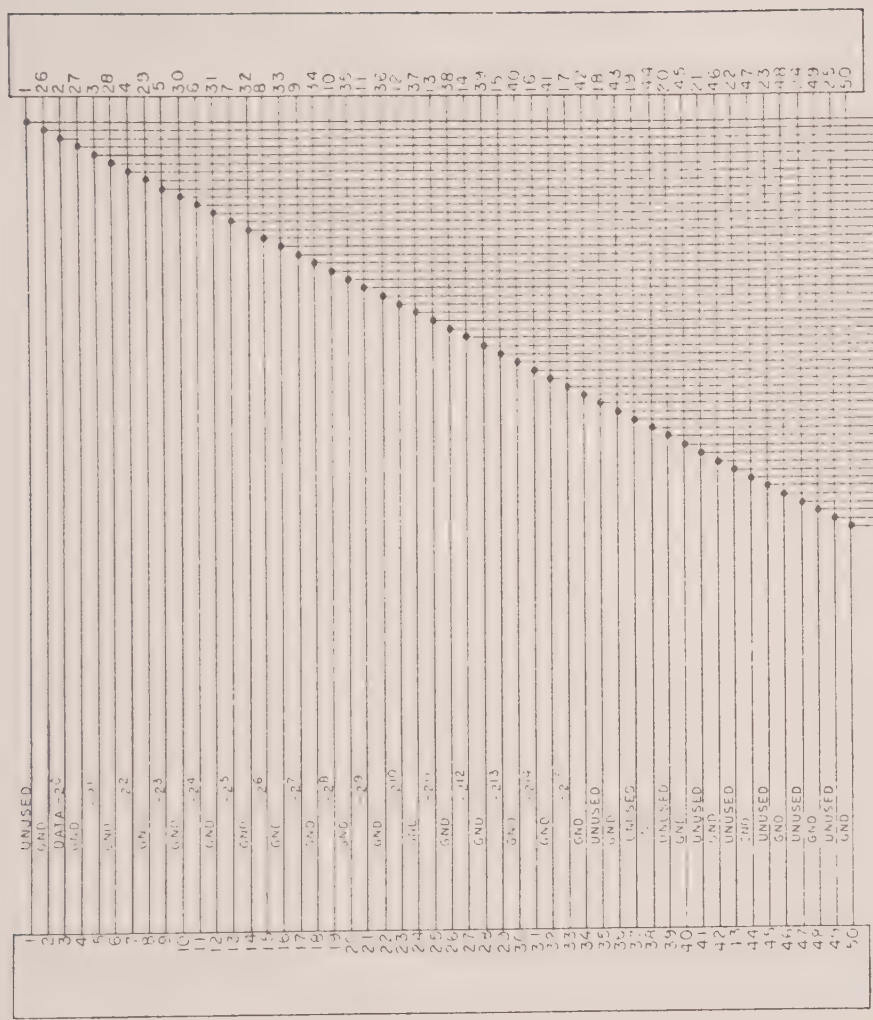


TO
J309-J1

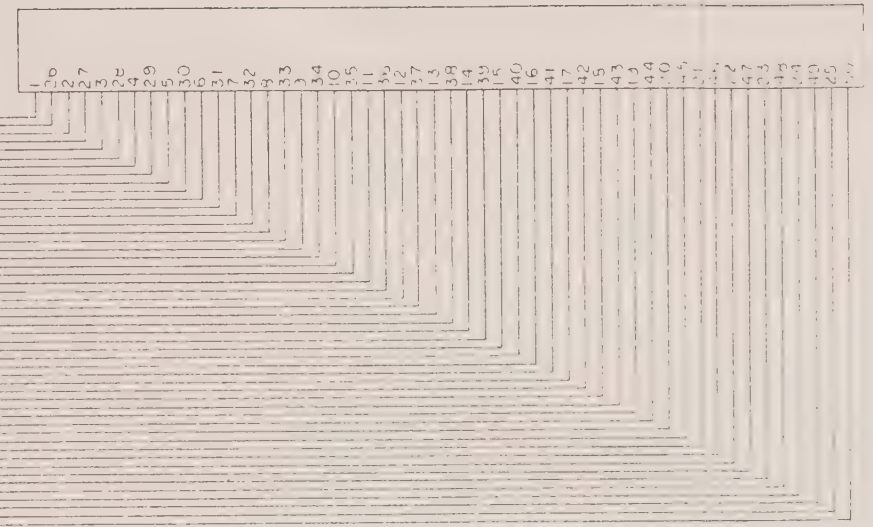
J110

J111

SCHEMATIC, 16 BIT
ADDRESS BUSS



PI
TO
J308-J1



SCHEMATIC, 16 BIT
DATA BUSS

APPENDIX C

OPTION 02 FRONT-PANEL CONTROLS

C-1 FREQUENCY

This set of switches controls the pulse repetition frequency from 005.0Hz to 49.95 MHz. The fourth digit is either 0 or 5, giving half steps between the steps of the third digit. The decimal point is positioned automatically, determined by the setting of the range switch (the rightmost thumbwheel switch in the group). The range switch reads directly in Hz, kHz, or MHz.

C-2 WIDTH

These switches control the pulse width, with settings of 010 ns to 9.99 ms allowable. The range switch reading directly in ns, μ s, or ms.

C-3 DELAY

The delay switches function in the same way as the WIDTH switches, controlling the time between the trigger output and the main pulse output in SINGLE pulse mode, or the spacing between the first and second pulses in DOUBLE pulse mode.

C-4 RAMPS

This set of switches consists of a common range switch with settings of $\times 3$ V/ns, V/ns, V/ μ s, or V/ms and separate LEADING EDGE and TRAILING EDGE three-digit switch sections. These switches control the *rate* or rise and fall—not the rise or fall times. The pulse amplitude must be taken into consideration to determine settings of a given rise or fall time.

C-5 AMPLITUDE

The AMPLITUDE switches are divided into three sections: 1) POLARITY, 2) RANGE, and 3) % OF RANGE. The POLARITY section consists of two switches. The first switch selects N (normal) or I (inverted); the second switch selects + (positive-going) or – (negative-going). The RANGE switch is effectively the attenuation control. The switch selects

full-scale (i.e., at maximum amplitude) ranges of 10.0 V, 5.00 V, 2.50 V, 1.25 V, .625 V, .312 V, .156 V, and .078 V. The % OF RANGE switches select the amplitude within the selected range, from 50.00% to 99.95%.

C-6 OFFSET

The OFFSET group of switches set the baseline offset with respect to ground. The first switch selects NEG (negative with respect to ground), POS (positive with respect to ground), and OFF (baseline at ground level). The second group of switches select the offset value from 0.000 V to 4.995 V. The fourth digit is either 0 or 5. It should be noted that the fourth digit in the FREQUENCY, AMPLITUDE, and OFFSET controls are provided for high resolution only; the basic accuracy and repeatability of the Model 1501A are unchanged.

C-7 PROGRAM MODE

The three PROGRAM MODE toggle switches allow local or remote (program) control of portions of the Model 1501A circuitry independently. This allows manual control of certain parameters while maintaining the others under external control. The three parameters which can be selected for local or remote control are CLOCK (pulse repetition frequency), D/W (delay and width) and OUTPUT (leading/trailing edge slope, polarity, normal/inverted, attenuation, amplitude, and offset).

C-8 CLOCK, GATE, AND PULSE MODE

These three toggle switches select internal or external clock, gated output either on or off by external signal, and single or double pulse. It should be noted that the internal/external clock switch, the gating mode switch, and the single/double pulse switch are enabled only when the appropriate local/remote switch is in the local position. For external/internal clock selection, the CLOCK switch must be in the local position. For gating and single/double pulse selection, the D/W switch must be in the local position.

ASSEMBLY NO. 350-21900DESCRIPTION MOD KIT/SERIAL FRONT PANEL CONTROLLER

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
	ADD	
*251-21049	Front Panel Assembly	
	DELETE	
251-21286	Front Panel Assembly	

ASSEMBLY NO. 350-21901DESCRIPTION MOD KIT/PARALLEL FRONT PANEL CONTROLLER

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
	ADD	
*251-21049	Assembly, Front Panel	
*249-21199	Sub Panel Rear Assembly	
	DELETE	
251-21286	Front Panel Assembly	
249-21283	Sub Panel Rear Assembly	

ASSEMBLY NO. 251-21049DESCRIPTION FRONT PANEL ASSEMBLY (DIGITSWITCH)

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
251-21205	Front Panel Assembly	
249-21206	Sub Panel, Front, Assembly	
401-22061	Front Panel Interface Board	

ASSEMBLY NO. 251-21205DESCRIPTION FRONT PANEL ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
250-21047	Front Panel	
630-00017	Switch, Toggle Mini	S202-207
630-00022	Switch, AC Power	S201

ASSEMBLY NO. 249-21206DESCRIPTION FRONT SUB PANEL ASSEMBLY

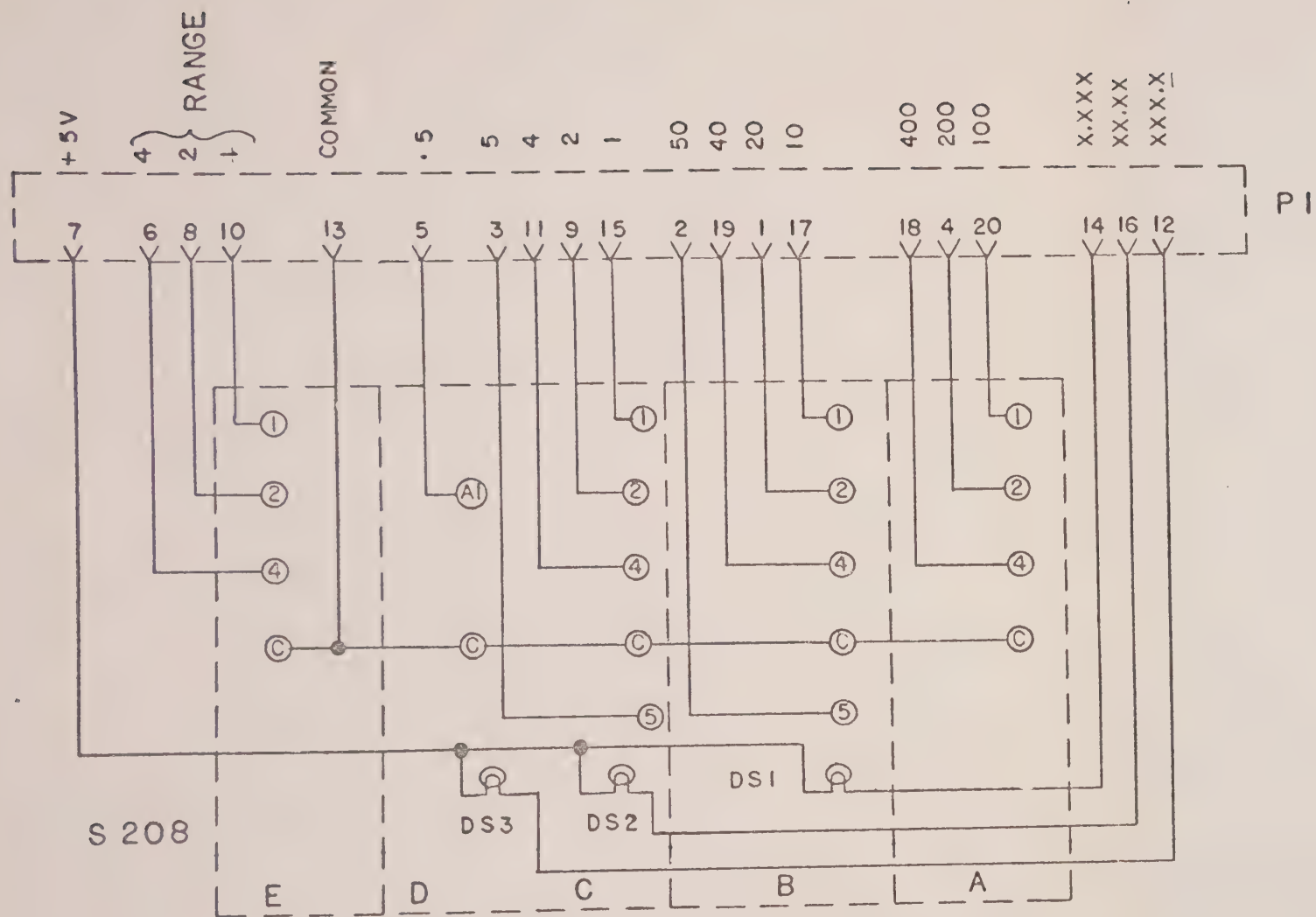
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
248-21050	Sub Panel	
	Standoff, HH Smith #8430	
635-22381	Switch Assy, EECO 201-445	S208
635-22382	Switch Assy, EECO 201-446	S209,210
635-22383	Switch Assy, EECO 201-447	S211
635-22384	Switch Assy, EECO 201-442	S212
635-22385	Switch Assy, EECO 201-440	S213
706-21204	(7) 20 Pin Cable, Assy, Flat Ribbon	
702-21200	Wire List, Sub Rear Panel Switches	Prod Ref
702-21201	Wire List, Front Panel	Prod Ref

ASSEMBLY NO. 401-22061DESCRIPTION FRONT PANEL INTERFACE BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22060	PC Board	
401-22061	Assembly Drawing	Prod Ref
140-22062	Schematic	Prod Ref
311-00074	Cap, Cerm .01 μ f	C1-8
318-00005	Cap, Tant 10 μ f 20V	C9
495-00054	Socket, IC 16 Pin	J1-7
595-00047	Resistor 4.7 Ω $\frac{1}{2}$ W 5%	R20
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R1-3
595-00471	Resistor 470 Ω $\frac{1}{2}$ W 5%	R14-19
595-00511	Resistor 510 Ω $\frac{1}{2}$ W 5%	R4-13
665-00037	IC MC 849P	IC7-48
665-00080	IC SN74145N	IC1,4-6
665-00100	IC SN75453N	IC 2,3
700-00127	Connector Transition 20 Pin Header 3M3428-2002	P1-7
706-21207	1/1 16 Pin Cable Assy Flat Ribbon	(P8-14)
706-21208	34 Pin Cable Assy Flat Ribbon	(J8)

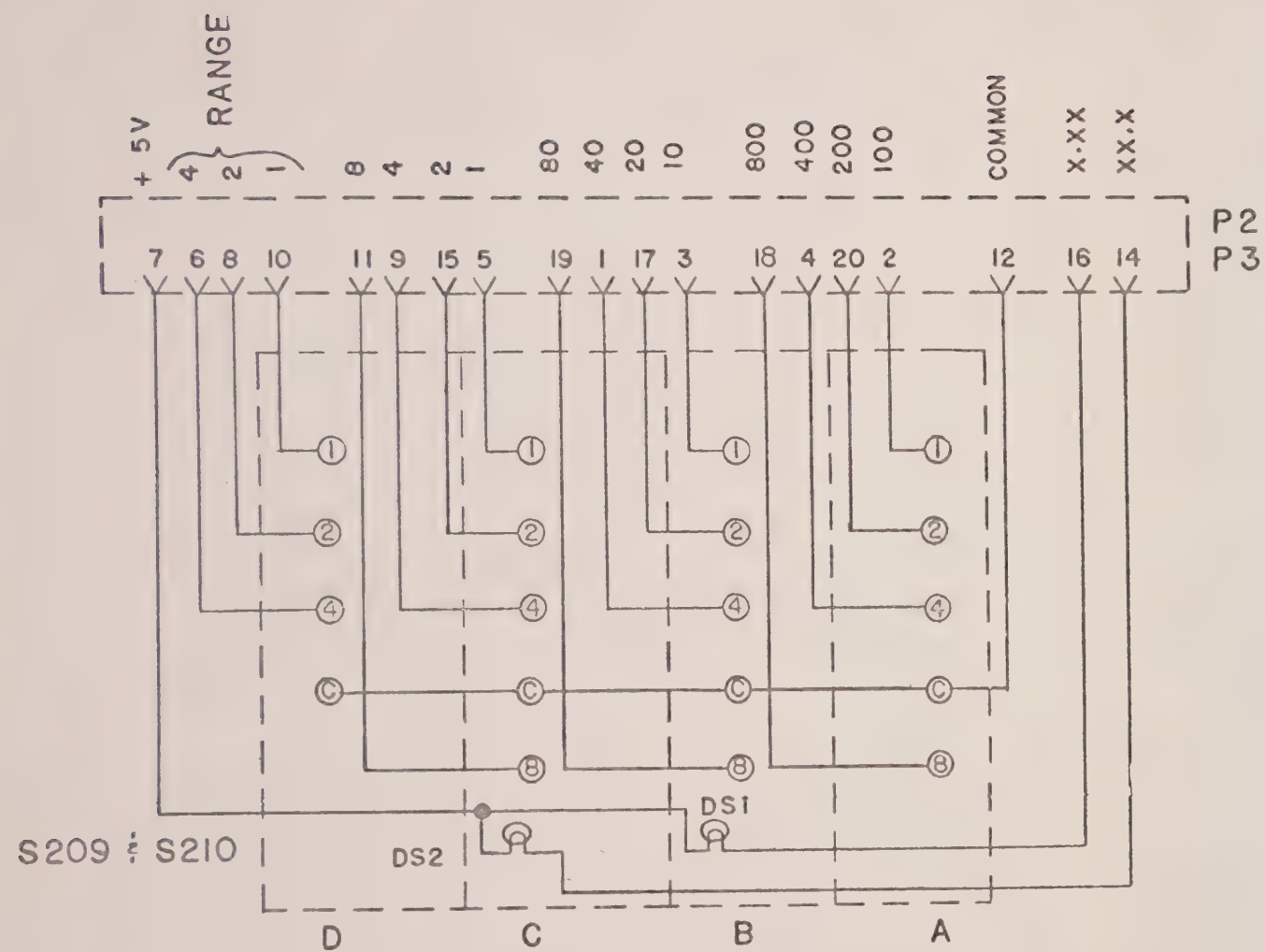
ASSEMBLY NO. 249-21199DESCRIPTION SUB PANEL , REAR, ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
248-21194	Panel	
144-21195	Silkscreen	Prod Ref
706-21202	Cable Assy, 50 Pin	J110
706-22625	Cable Assy, 50 Pin	J111
706-21203	Cable Assy, 20 Pin	J112
201-00004	Screw #3-48x $\frac{1}{2}$ BHMS (6)	Prod Ref
215-00002	Lockwasher #3 (6)	Prod Ref
240-00019	Hex Nut #3-48 (6)	Prod Ref
460-00003	Solder Lug #4 (1)	Prod Ref
758-00301	Wire, Bare Buss	Prod Ref
793-00315	Sleeving TFE #15	Prod Ref



CABLE AND SWITCH ASSY.
FREQUENCY

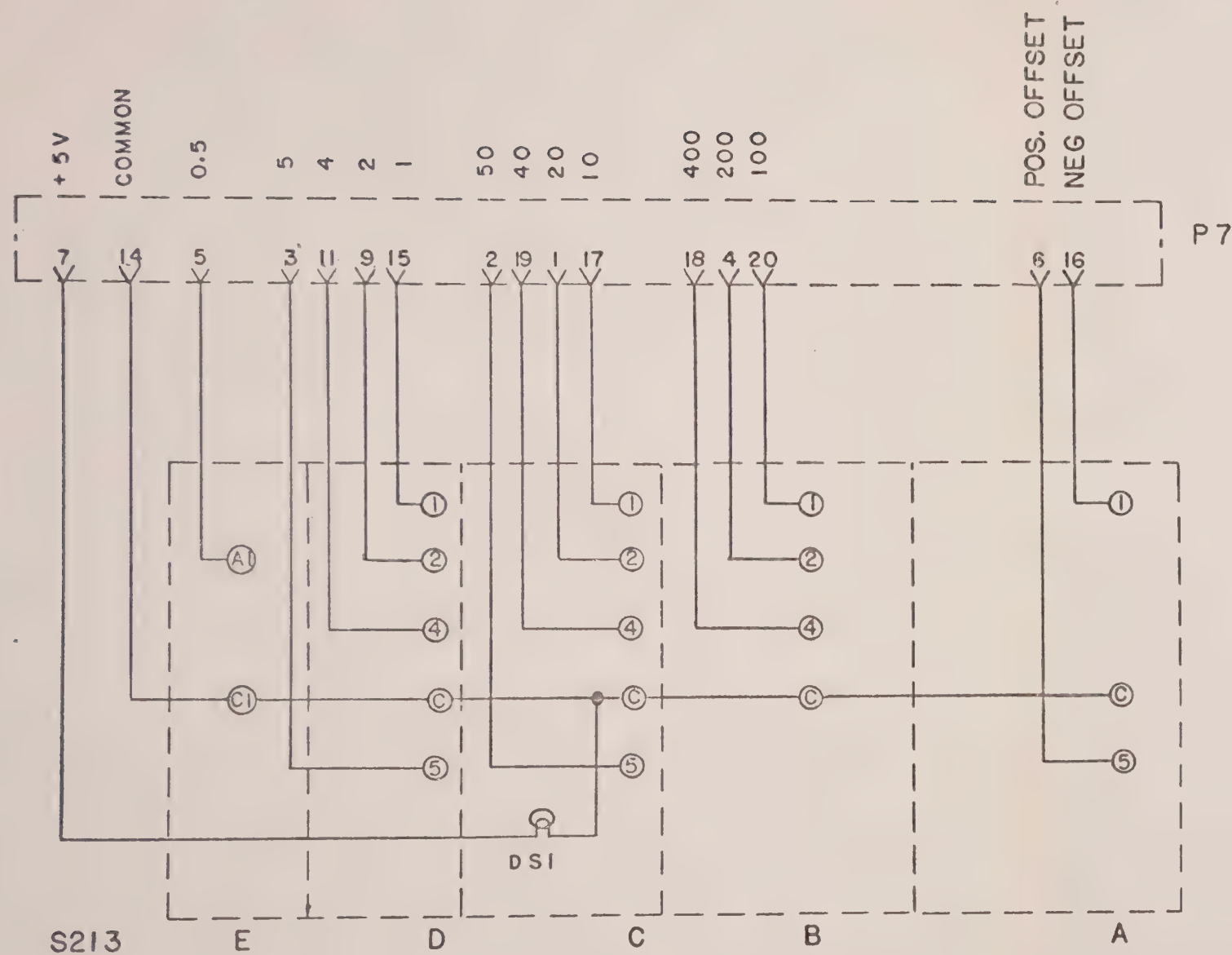
MODEL 1501-3
640-
B-21220 C



CABLE AND SWITCH ASSY.
DELAY AND WIDTH

WIRE LIST - 702-21201

MODEL 1501-3
640-
B-21221 C



CABLE AND SWITCH ASSY.
OFFSET

WIRELIST 702-21201

MODEL 1501 - 3

B-640-
21224 B

APPENDIX D

OPTION 01 SOPI

SERIAL-BY-WORD ISOLATED

D-1 GENERAL.

Programming the Model 1501A consists of addressing a function and writing the function data into the internal program storage. The function address consists of three bits forming the BCD values one through seven to conform to the function values listed in Table D-1. The data word for each address (each function) must consist of 16 bits. Each word consists of one bit for mode control, three bits for range selection, and 12 bits for three digits of vernier control. Table D-2 gives the range values, and Table D-3 lists the data and address input/output pin connections.

D-2 PROGRAMMING SPECIFICATIONS.

a. **Format.** Serial-by-word program format with three-bit function address and 16-bit data word.

b. **Logic Levels.** Positive true; logic "0" 0 to +0.5V; logic "1", +4.5 to +5V. Input logic uses separate address and data feedthrough connectors on rear panel. Logic lines optically isolated from internal chassis ground and internal voltage references.

Logic lines require +5V operating power from external source. Current requirements approximately 10ma per bit when bits are in a logic "0" state.

c. **Vernier Programming.** Each set of vernier connections is made up of three digits in 8-4-2-1 BCD form. Width and delay programming is straightforward; the number programmed in BCD form is the required value. For example, a pulse width of 172 μ s is a vernier value (in BCD) of 172. Frequency, amplitude, and offset require transformation from the desired value to the correct vernier. These functions will be discussed in the following paragraphs.

d. **Frequency Programming.** Because the frequency ranges do not have end points which are even decades, the required vernier is found by multiplying the desired frequency by a factor of two and taking the three most significant digits as the vernier. For example, a pulse repetition frequency of 452.3kHz multiplied by two gives a value of 904.6 and a vernier program of 905.

e. **Amplitude Programming.** The basic (unattenuated) amplitude range is 5 V with 000 vernier and 9.99 V with 999 vernier. To determine the vernier for a given amplitude, including attenuation, use the formula below:

$$\text{Ampl. Vernier} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005}$$

f. **Offset Programming.** The range of offset programming is from 0 to 5 V. The vernier program is the required offset value in volts, multiplied by 200. For example, if the required offset is 200 mV, the vernier is 200 x 0.2, or 040.

g. **Leading and Trailing Edge Ramps.** Since the leading and trailing edge ramps of the Model 1501A are constant slope with respect to changes in amplitude vernier, and constant risetime with respect to changes in attenuation, a calculation must be made to determine the program for a given combination of amplitude and rise/fall time. The *fastest* leading and trailing edge times are obtained at a vernier of 999, and the *slowest* times at a vernier of 100. To determine the proper vernier, use the following formula:

$$\text{Ramp Rate} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{rise or fall time}}$$

Where "K" = .8 for 10-90%, K = .6 for 20-80%, etc.

SAMPLE PROGRAM

Required Amplitude: 800 mV

Required 10-90% risetime: 20 ns

Step 1. Determine attenuation value by inspecting Table D-2. An 800 mV output will be obtained on Range 4 which has an attenuation value of 8.

Step 2. Set attenuator to Range 4.

Step 3. Determine amplitude vernier setting using the attenuation value found in Step 1.

$$\begin{aligned} \text{Ampl. Vernier} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005} \\ &= \frac{(.800) \times (8) - 5}{.005} \\ &= 280 \end{aligned}$$

Step 4. Set Amplitude vernier to 280.

Step 5. Determine ramp rate using:

$$\begin{aligned}
 \text{Ramp Range} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{risetime}} \\
 &= \frac{(.800) \times (8) \times .8}{20 \text{ ns}} \\
 &= \frac{5.12 \text{ V}}{20 \text{ ns}} \\
 &= \frac{5.12 \text{ V}}{.02 \mu\text{s}} \\
 &= 256 \text{ V}/\mu\text{s}
 \end{aligned}$$

By inspecting Table D-2, we find that a ramp rate of 256 V/ μ s can be obtained with Ramp Range = 1.

Step 6. Set Ramp Range to 1.

Step 7. Set Ramp vernier to 256.

NOTE

Since the vernier only varies between counts of 100 to 999, it may be necessary to multiply the Ramp Rate by either 10 or 100 to obtain the three-digit vernier setting. Example: if Ramp Rate = 24 V/ μ s, then Vernier = 24 x 10 = 240. Example: if Ramp Rate = 1.3 V/ μ s, then Vernier = 1.3 x 100 = 130.

D-3 RESET MODES

When primary power is turned on, all internal storage is reset to zero, and the Model 1501A is in the following modes: maximum attenuation, inverted pulse mode, negative pulse, zero offset, Gate Off mode, frequency, delay, width, rise and fall times at minimum, internal clock, and single pulse. After initial programming, reset of internal storage can be accomplished by activating the Master Reset line on pin 1 of rear-panel connectors J110/J111. Master Reset is activated in the low state.

D-4 DATA AND ADDRESS TIMING

Timing of data/address and strobe inputs are shown in figure D-1.

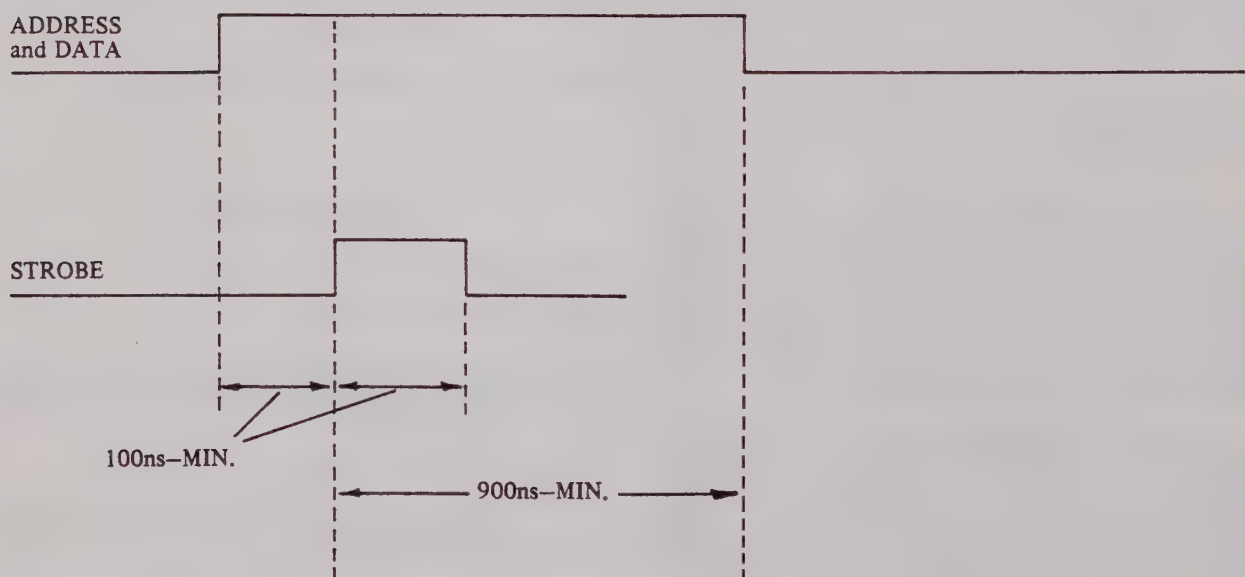


Figure D-1 Timing

Table D-1. Function Address and Data Input

Function	Address			16-Bit Data Word				
	2 ²	2 ¹	2 ⁰	Mode bit 2 ¹⁵	Range Char. 2 ¹⁴ 2 ¹³ 2 ¹²			3 BCD Digits Vernier 2 ¹¹ — 2 ⁰
Frequency	0	0	1	int/ext	Table D-2			
Delay	0	1	0	sgl/dbl	Table D-2			
Width	0	1	1	inv/norm	Table D-2			
Ldg Edge*	1	0	0	gate off/gate on	Table D-2			
Trlg Edge*	1	0	1	not used	not used			
Offset	1	1	0	not used	0 1 0 = pos, 1 0 0 = neg			
Amplitude	1	1	1	neg/pos	Attenuation			
				pulse pol	Table D-2			

Table D-2. Range Programming

Function	Range Value	Range	Vernier
Frequency	0	0.5 Hz-4.995 Hz	100-999
	1	5 Hz-49.95 Hz	100-999
	2	50 Hz-499.5 Hz	100-999
	3	500 Hz-4.995 kHz	100-999
	4	5 kHz-49.95 kHz	100-999
	5	50 kHz-499.5 kHz	100-999
	6	500 kHz-4.995 MHz	100-999
	7	5 MHz-49.95 MHz	100-999
Delay/Width	0	10 ns-99.9 ns	100-999
	1	100 ns-999 μ s	100-999
	2	1 μ s-9.99 μ s	100-999
	3	10 μ s-99.9 μ s	100-999
	4	100 μ s-999 μ s	100-999
	5	1 ms-9.99 ms	100-999
	6	10 ms-99.9 ms	100-999
	7	100 ms-999 ms	100-999
Ramp Rate	0	uncalibrated range*	100-999
	1	0.1-0.999 V/ns	100-999
	2	10.0-99.9 V/ μ s	100-999
	3	1.0-9.99 V/ μ s	100-999
	4	0.1-0.999 V/ μ s	100-999
	5	10.0-99.9 V/ms	100-999
Attenuation	0	(x 128) 40-80 mV	000-999
	1	(x 64) 80-156 mV	000-999
	2	(x 32) 156-312 mV	000-999
	3	(x 16) 312-625 mV	000-999
	4	(x 8) 0.62-1.25 V	000-999
	5	(x 4) 1.25-2.5 V	000-999
	6	(x 2) 2.5-5.0 V	000-999
	7	(x 1) 5.0-10.0 V	000-999

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table D-3. Address and Data Input

ADDRESS - J110 and J111			
Pin	Signal	Pin	Signal
1	Master Reset	22	Gate Mode
2	2 ⁰ Addr. Bit	23-24	Not used
3	2 ¹ Addr. Bit	25	+5 V input-LED common
4	2 ² Addr. Bit	26-41	Logic Common (not tied to chassis ground)
5-18	not used		
19	Strobe	42-49	Open - may be used for feedthrough signals
20-21	not used	50	+5 V input-LED common
DATA - J112 and J113			
Pin	Signal	Pin	Signal
1	not used	18-24	not used
2	2 ⁰	25	+5 V input-LED common
3	2 ¹	26-41	Logic Common (not to chassis ground)
4	2 ²	42-49	Open - may be used for feedthrough signals
5	2 ³	50	+5 V input - LED common
6	2 ⁴		
7	2 ⁵		
8	2 ⁶		
9	2 ⁷		
10	2 ⁸		
11	2 ⁹		
12	2 ¹⁰		
13	2 ¹¹		
14	2 ¹²		
15	2 ¹³		
16	2 ¹⁴		
17	2 ¹⁵		

ASSEMBLY NO. 350-21909DESCRIPTION MOD KIT/ LED ISOL. - 3 BIT ADDRESS, 16 BIT DATA
POS. TRUE LOGIC

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
	-ADD-	
401-20666	3 Bit Isolated Bd. Assy	J309
401-21484	S1 Isolated Interface Bd. Assy	J308
401-22619	Serial D/A Board Assy	J305-307 311-314
249-21385	Sub Panel Rear Assy	
	-Add to 820-21290 -	
146-26042	Doc List	Prod Ref
700-00034	Connector, 50 Pin Amphenol	
	-DELETE-	
401-21212	Parallel D/A Bd. Assy	J305-307 311-314
249-21283	Sub Panel Rear Assy	
	DELETE FROM 820-21290	
700-00024	Connector, 24 Pin Amphenol	

ASSEMBLY NO. 401-20666DESCRIPTION ISOLATED 3 BIT ADDRESS BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-21480	PC Board	
401-20666	Assembly Drawing	Prod Ref
140-20667	Schematic	Prod Ref
311-00041	Cap, Cerm .1 μ f 12V	C1, 3, 5
318-00001	Cap, Tant 47 μ f 20V	C2
318-00005	Cap, Tant 10 μ f 20V	C4
335-00022	Choke 1 μ h	L1
376-00022	Diode, 1N4448	CR1
595-00102	Resistor 1K 1/4W 5%	R8, 16-19, 23-29
595-00103	Resistor 10K 1/4W 5%	R20
595-00331	Resistor 330 Ω 1/4W 5%	R21, 22
595-00391	Resistor 390 Ω 1/4W 5%	R2-6
595-00511	Resistor 510 Ω 1/4W 5%	R9-12
595-00512	Resistor 5.1K 1/4W 5%	R13

ASSEMBLY NO. 401-20666DESCRIPTION ISOLATED 3 BIT ADDRESS BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
663-00124	Transistor 2N4401	Q1
665-00053	IC MC3000P	IC 5
665-00123	IC MC4038P	IC 6
665-00154	IC MC7242P	IC 2
665-00210	LED HP 5082-4360	IC1, 3, 4, 7, 9
700-00144	Header, 3M 50 Pin 3433-2002	J1

ASSEMBLY NO. 401-21484DESCRIPTION S-1 INTERFACE ISOLATED BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-21483	PC Board	
401-21484	Assembly Drawing	Prod Ref
140-21485	Schematic	Prod Ref
311-00007	Cap, Cerm 100pf 1KV 10%	C9,10
311-00009	Cap, Cerm 500pf 1KV 10%	C8,11
311-00035	Cap, Cerm 15pf 1KV 10%	C7
311-00041	Cap, Cerm .1 μ f 12V	C1
311-00074	Cap, Cerm .01 μ f 100V	C2-6 12-15
318-00005	Cap, Tant 10 μ f/20V	C2
335-00022	Choke 1 μ h	L1
376-00022	Diode, 1N914B	CR1
551-00041	Potentiometer 5K 89PR	R1
595-00101	Resistor 100 Ω $\frac{1}{4}$ W 5%	R25,28
595-00102	Resistor 1K $\frac{1}{4}$ W 5%	R18-22
595-00152	Resistor 1.5K $\frac{1}{4}$ W 5%	R27

ASSEMBLY NO. 401-21484DESCRIPTION S-1 INTERFACE ISOLATED BOARD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00221	Resistor 220 Ω $\frac{1}{2}$ W 5%	R24
595-00391	Resistor 390 Ω $\frac{1}{2}$ W 5%	R2-17
595-00512	Resistor 5.1K $\frac{1}{2}$ W 5%	R23,26
595-00511	Resistor 510 Ω $\frac{1}{2}$ W 5%	R29-44
665-00053	IC MC3000P	IC 15,24
665-00078	IC MC3004P	IC 25
665-00084	IC MC3022P	IC3,10,18 23,26
665-00130	IC MC8601P	IC 1
665-00110	IC MC3002	IC 16
665-00054	IC MC3061P	IC 2,8
665-00145	IC MC8309P	IC9,17
376-00094	LED, HP 5082-4360	IC4-7,11- 14,19-22 27-30
700-00144	Header, 50 Pin, 3M 3433-2002	J1

ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
400-22618	PC Board	
401-22619	Assembly Drawing	Prod Ref
140-22620	Schematic	Prod Ref
311-00001	Cap, Cerm 10pf 1KV	C3
311-00074	Cap, Cerm .01 μ f 100V	C2,5,6, 8,9
318-00004	Cap, Tant 27 μ f 10V	C1
318-00005	Cap, Tant 10 μ f 20V	C4,7
335-00022	Choke 1.0 μ h	L1
495-00054	Socket, IC 16 Pin	J1
551-00039	Potentiometer 200 Ω 89PR	R30
551-00040	Potentiometer 1K 89PR	R27
595-00100	Resistor 10 Ω $\frac{1}{2}$ W 5%	R28,33
595-00153	Resistor 15K $\frac{1}{2}$ W 5%	R32
595-00165	Resistor 1.6M $\frac{1}{2}$ W 5%	R11
595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R13-24
595-00335	Resistor 3.3M $\frac{1}{2}$ W 5%	R12
595-00394	Resistor 390K $\frac{1}{2}$ W 5%	R9
595-00512	Resistor 5.1K $\frac{1}{2}$ W 5%	R34,35

ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
595-00824	Resistor 820K $\frac{1}{2}$ W 5%	R10
611-00001	Resistor 4K .05%	R1
611-00002	Resistor 8K .1%	R2
611-00003	Resistor 16K .1%	R3
611-00004	Resistor 32K .1%	R4
616-00015	Resistor 165K 1/8W 1% MF	R7
616-00016	Resistor 316K 1/8W 1% MF	R8
616-00017	Resistor 3.32K 1/8W 1% MF	R25
616-00325	Resistor 4.22K 1/8W 1% MF	R31
616-00330	Resistor 6.19K 1/8W 1% MF	R26
616-00332	Resistor 9.09K 1/8W 1% MF	R29
616-00342	Resistor 40.2K 1/8W 1% MF	R5
616-00347	Resistor 80.6K 1/8W 1% MF	R6
663-00070	Transistor 2N3904	Q1-12
665-00078	IC MC3004P	IC 5
665-00079	IC N5741CT	IC 8
665-00110	IC MC 3002P	IC 12

ASSEMBLY NO. 401-22619DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

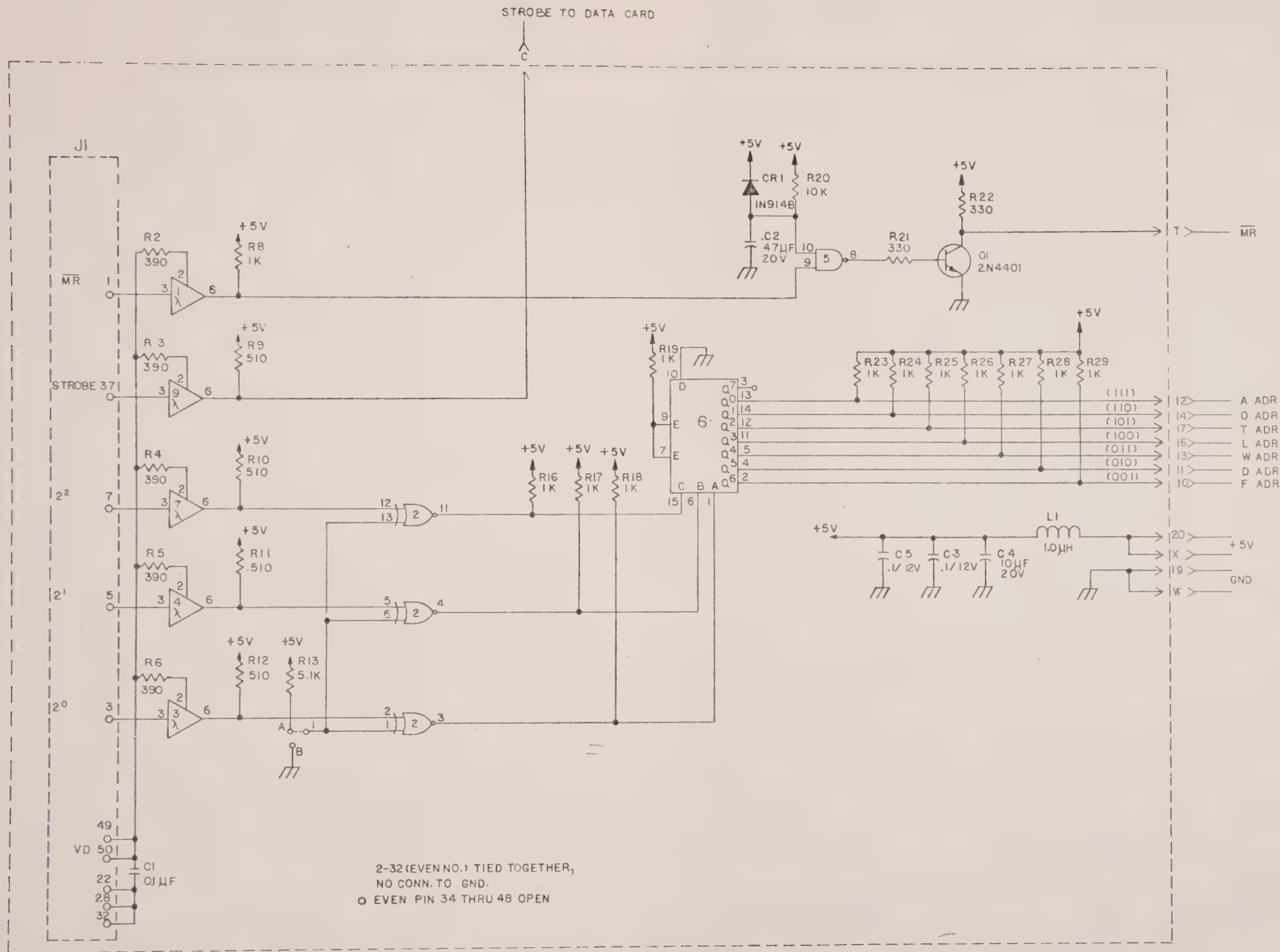
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
665-00112	IC MC 3008P	IC 13
665-00144	IC MC 4015P	IC9-11,14
665-00151	IC MC 4002P	IC 4
665-00145	IC MC 8309P	IC 6,7
665-00152	IC N8266B or MC7266P	IC 15
665-00153	IC N74157B or MC74157P	IC 1-3
495-00027	Amp Pins	XIC8
496-00043	Transistor Pad	XIC8

ASSEMBLY NO. 249-21385DESCRIPTION ASSEMBLY SUB-PANEL REAR

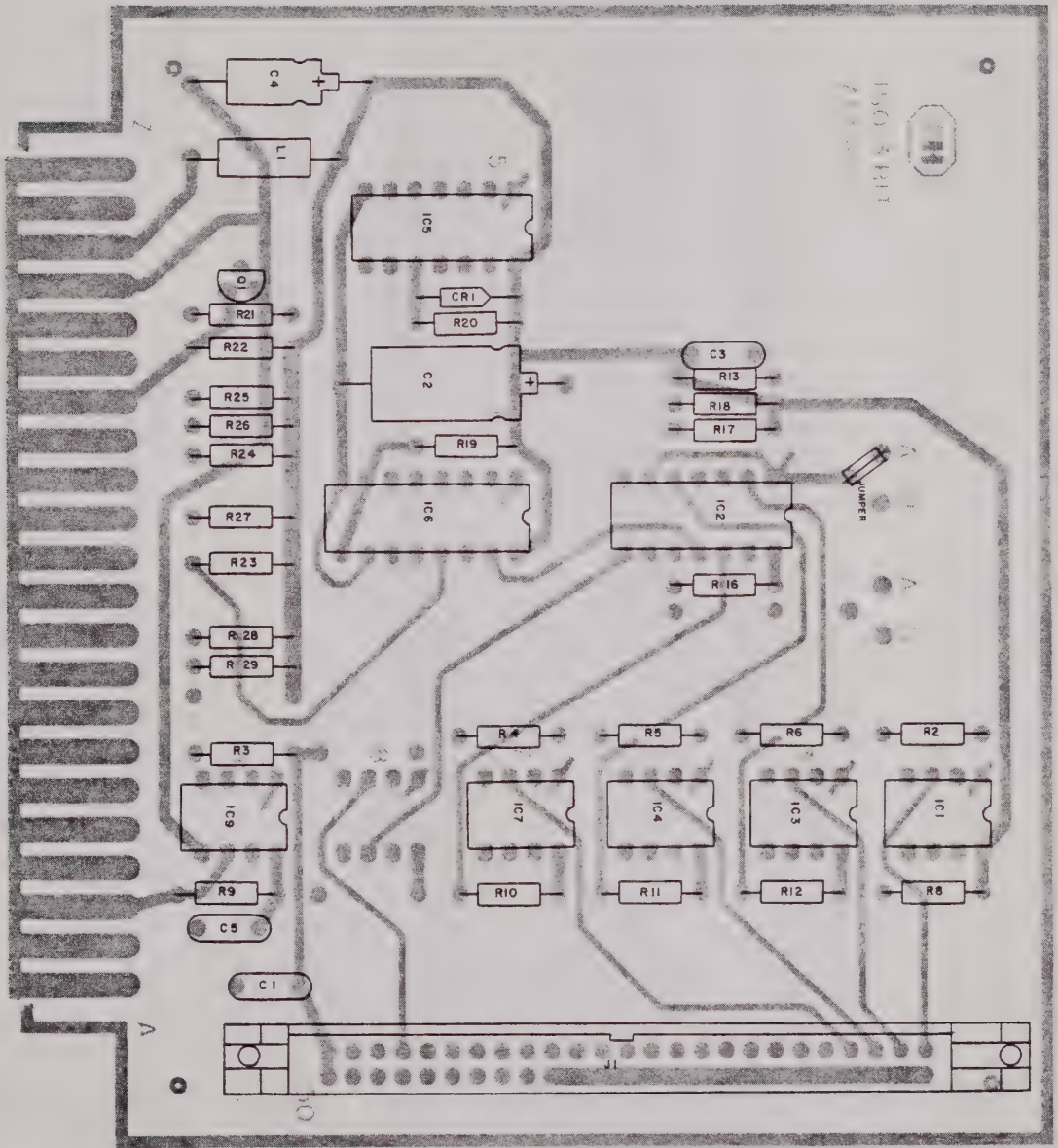
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
248-21381	Panel	
144-21383	Silkscreen, Panel	Prod Ref
706-21379	Cable Assy, Dual 50 Pin	J112,J113
706-21380	Cable Assy, Dual 50 Pin	J110,J111
201-00004	Screw, 3-48x $\frac{1}{2}$ BHMS (8)	Prod Ref
215-00002	Lockwasher #3 (8)	Prod Ref
240-00019	Hex Nut #3-48 (8)	Prod Ref

ASSEMBLY NO. 820-21290DESCRIPTION STANDARD ACCESSORIES

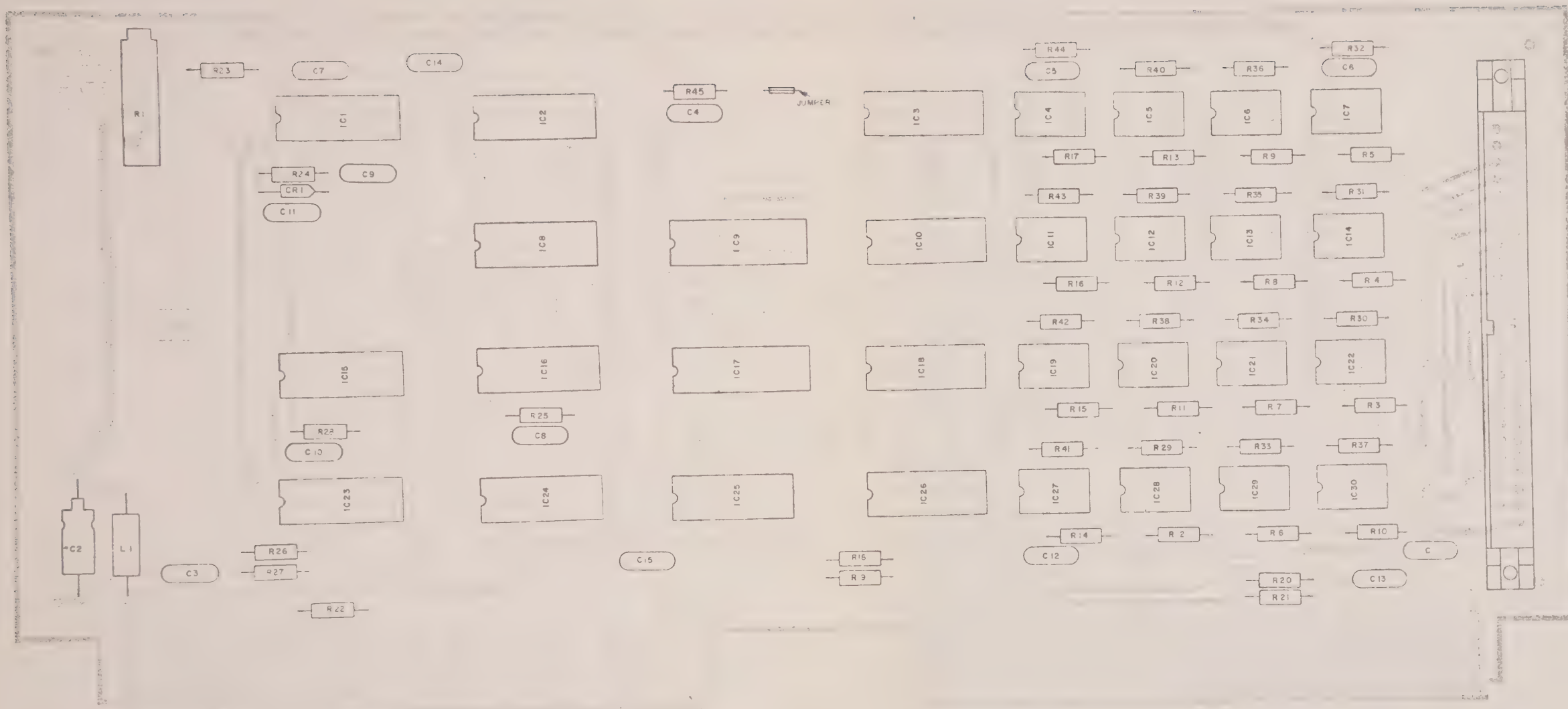
ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.
148	Manual	
786-00002	Power Cord	
800-00032	Envelope	
700-00034	Amphenol, 50 Pin Connector	
700-00024	Connector, 24 Pin Amphenol	
401-23973	Extender Bd Assy 44 Pin	Optional
401-23975	Extender Bd Assy 88 Pin	Optional



SCHEMATIC, ISO.
3 BIT ADDRESS BOARD
(J 309A)

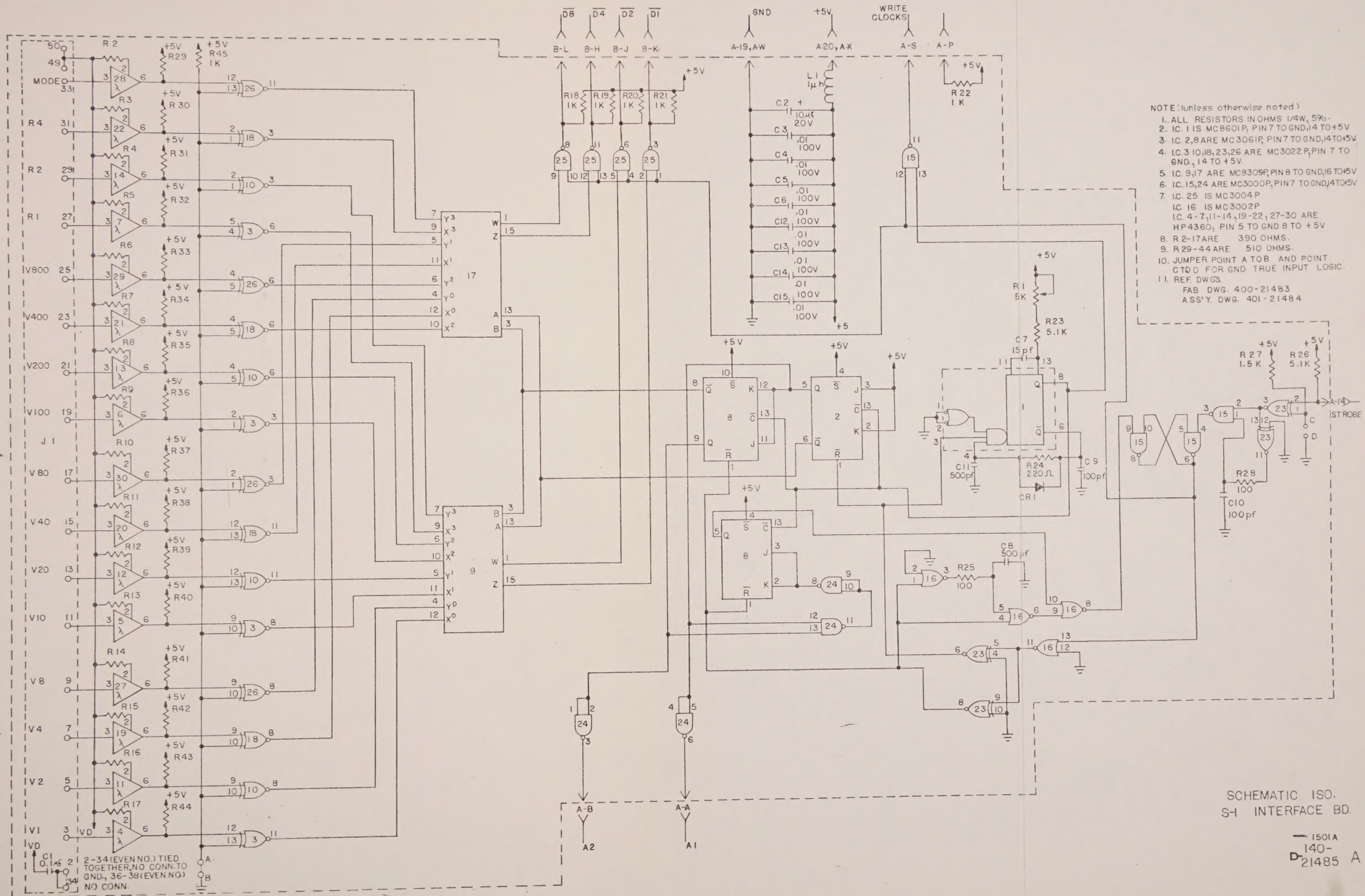


ASSEMBLY DRAWING
ISO. 3 BIT ADDRESS



ASSEMBLY DRAWING
ISO. S - I
INTERFACE

1501 A
D 401-
21484 B



CHANGE INFORMATION

The following types of changes are found in this Section:

Corrections—

changes due to errors in text or illustrations

Additions—

new text or new illustrations to supplement original manual

Revisions—

new text or new illustrations to up-date original manual

Options—

information on non-standard accessories or options available for this instrument

Modifications—

information on special features of a custom-designed instrument

